iPLUG

Deliverable D3.2

Prototype Development, Experimental Validation, and Evaluation of LV Multiport Converters

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Author	Ahmed Yahia Farag Abdelfattah, Paolo Mattavelli, Khaled Awadallah Ahmed Mohamed (UNIPD) Mohammed Debbat (IREC)

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Typhoon HIL	Sergio Costa Milan Arsenijevic
CTH	Mebtu Beza

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List of Acronyms

4-W	Four-Wire
ac	Alternating Current
ADC	Analog-to-Digital Converter
BPF	Band-Pass Filter
CMV	Common-Mode Voltage
CSC	Current Source Converter
CSPI	Cooling System Performance Index
dc	Direct Current
DER	Distributed Energy Resource
DN	Distribution Network
EMI	Electromagnetic Interference
ESR	Effective Series Resistance
ESS	Energy Storage System
ESOP	Enhanced SOFT Open Point
EV	Electric Vehicle
EU	European Union
FFS	Fixed-Frequency Sampling
FPGA	Field Programmable Gate Array
LDO	Low Drop-Out (Regulator)
LED	Light Emitting Diode
LFR	Loss-Free Resistor
LPF	Low-Pass Filter
MG	Microgrid
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPC	Multiport Converter
MOO	Multi-Objective Optimization
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
POPI	Power Output Port Interface
PFC	Power Factor Correction
PV	Photovoltaic
PWM	Pulse-Width Modulation
RC	Resistor-Capacitor

RES	Renewable Energy Source
RCP	Rapid Control Prototyping
RMS	Root Mean Square
RTOS	Real-Time Operating System
SMC	Sliding-Mode Control
SiC MOSFET	Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistor
THD	Total Harmonic Distortion
TSSOP	Thin Shrink Small Outline Package
VCO	Voltage-Controlled Oscillator
VSC	Voltage Source Converter
WP	Work Package
ZVS	Zero-Voltage Switching

List of Nomenclatures

C_f	Input capacitor
C_{dc1}, C_{dc2}	dc capacitor connected to port 1 and port 2, respectively
d_{Bu_x}	Duty cycle of the buck half-bridge
$d_{Bo_{a1}}$	Duty cycle of the first boost half-bridge
$d_{Bo_{a2}}$	Duty cycle of the second boost half-bridge
ΔP_1	Power step size for Port 1
ΔP_2	Power step size for Port 2
E_{on}	Turn-on switching energy loss
E_{off}	Turn-off switching energy loss
f_{sw}	Switching frequency
i_a	AC grid current at phase a
i_b	AC grid current at phase b
i_c	AC grid current at phase c
$i_{Cf,a}$	Current through the input capacitor of module a
$i_{La1,av}$	Average inductor current of inductor L_1 in module a
$i_{La2,av}$	Average inductor current of inductor L_2 in module a
L_1, L_2	Main Inductors of dc port 1 and dc port 2, respectively
L_f	Grid-side filter inductor
P_{ac}	Fixed ac port power
P_{dc}	Total power to dc side
P_{dc1}	Power at dc Port 1
P_{dc2}	Power at dc Port 2
$P_{\text{dc,rated1}}$	Rated power of dc Port 1
$P_{\text{dc,rated2}}$	Rated power of dc Port 2
$P_{\text{op}}(t)$	Instantaneous operating power
$P_{\text{PV}}(t)$	PV power profile over time
$P_{\text{storage}}(t)$	Power at storage port
P_x	Power delivered by module x ($x = a, b, c$)
P_{fe}	Iron losses in inductors
P_{cu}	Copper losses in inductors
P_{cond}	Semiconductor conduction losses
P_{sw}	Semiconductor switching losses
P_{ac}	Total power from ac side
R_{DS}	on-state resistance of MOSFET
r_x	Emulated input resistance of module x

T_j	Semiconductor junction temperature
V_{DS}	Drain-source voltage
$V_{\text{RMS}x}$	RMS value of phase voltage x
V_{dc}	DC-side voltage
V_{dc1}	DC voltage at port 1
V_{dc2}	DC voltage at port 2
V_{off}	Offset voltage
$\hat{I}_m$	Peak phase current
$\hat{I}_{m1}$	Equivalent reference peak phase current from DC MG#1
$\hat{I}_{m2}$	Equivalent reference peak phase current from DC MG#2
$\hat{V}_m$	Peak value of AC grid phase voltage
ω	AC grid angular frequency (rad/s)
θ_x	Phase angle of voltage v_x
v_x	AC grid phase voltage at $x \in \{a, b, c\}$
v_{am}, v_{bm}, v_{cm}	AC-side module voltages for modules a, b, and c

1 Executive Summary

The EU's commitment to net-zero greenhouse gas emissions by 2050 necessitates rapid deployment of power converter-interfaced devices in electric power systems. This includes renewable energy sources (RESs) and energy storage systems (ESSs) in distribution networks (DNs). Traditional two-port power converters often fail to meet demand profiles effectively, leading to significant voltage fluctuations during generation-demand imbalances, particularly in radial feeders.

Multiport Converters (MPCs) provide an effective solution by integrating multiple energy ports into a single aggregated hub, offering high controllability and efficient energy management across all ports while maintaining power quality and grid stability. MPCs can address DN challenges by reducing conversion stages, leading to cost-efficiency and higher power density. MPCs offer flexibility in selecting the number of ports and their characteristics (AC or DC), making them ideal energy hubs for connecting feeders, substations, RESs, and ESSs. Compared to conventional systems composed of multiple individual interfacing converters, MPCs provide lower system cost, reduced size, and higher power density. Advanced controllability, communication, and computational capabilities in MPCs support future smart grids by decentralizing decision-making processes, enabling rapid responses, and holistic control to enhance overall grid performance.

WP3 focuses on investigating and enabling MPCs in low-voltage (LV) DNs, addressing challenges such as developing efficient and compact circuit topologies for interfacing three-phase and single-phase AC systems with multiple DC ports. This will enhance converter efficiency, improve power density, and reduce component counts by minimizing conversion stages. Additionally, control and modulation constraints will be addressed to ensure Zero-Voltage-Switching (ZVS) and reduce passive reactive elements to boost power density. High-performance current and voltage control techniques will maintain control bandwidth and impedance passivity across all ports, reducing dynamic instability and transient oscillations in future distribution grids.

At the distribution level, DNs with significant penetration of renewable sources and various industrial loads require power electronics to facilitate the integration of renewables and ESSs, optimize network use, and connect loads at different voltage levels. Power-electronic solutions like ESOP, smart transformers, and MPCs enhance capacity, flexibility, and controllability in distribution grids. For residential areas, MPCs accommodate future connections of EVs and distributed renewable generation, improving load balance, voltages, and renewable capacity.

In household settings, MPCs link local RESs and ESSs with the distribution grid, supporting local energy storage systems and EVs. This enhances system efficiency and reduces

integration costs, optimizing energy management at the household level and contributing to the overall stability and efficiency of the distribution network.

This report, Deliverable 3.2 of the iPlug project, provides a comprehensive overview of the laboratory prototypes developed and the experimental validation conducted as part of WP3, which focuses on the investigation of multiport converters (MPCs) for LV applications. Building upon the foundations laid in the previous WP3 deliverable, D3.1 [1], which introduced innovative single-stage non-isolated MPC topologies tailored for residential use, this report emphasizes the experimental assessment of those proposed converter architectures under a wide range of realistic operating conditions.

In Sections 3 and 4, the experimental tests to validate the performance and efficiency of the proposed converters under steady-state and dynamic scenarios are presented, reflecting practical grid-interfacing and energy management requirements. Furthermore, this deliverable advances the evaluation of MPCs by incorporating a multi-objective optimization framework. The optimization simultaneously targets high efficiency and elevated power density—two critical metrics for compact and cost-effective power conversion systems. The results demonstrate the ability of MPCs to meet stringent performance targets while reducing the component count and enhancing system integration.

In Section 5, a comparative study is presented between the proposed MPCs and conventional solutions based on multiple interconnected two-port converters. Under mission profiles emulating renewable energy generation and storage, the MPCs consistently outperformed their counterparts, particularly in terms of system-level efficiency and compactness.

Finally, the report details the refinement and validation of a non-linear control strategy originally proposed in D3.1 [1] for the Y-converter topology in Section 6. The enhanced control approach has been extended and adapted for the broader class of MPCs introduced in this work. Its effectiveness is demonstrated through improved transient response, robustness against parameter variations, and overall control performance under varied operating conditions.

2 Introduction

2.1 Background and Motivations for Multiport Converters

The urgency of the climate crisis, coupled with the European Union's strategic goal of achieving climate neutrality through net-zero greenhouse gas emissions by 2050, is accelerating the deployment of power converter-interfaced devices within electric power systems. This growing reliance on power electronics, particularly for integrating renewable energy sources (RESs) and energy storage systems (ESSs) into distribution networks (DNs), introduces new operational challenges that demand innovative converter architectures and control strategies to ensure both efficiency and grid reliability [2].

Traditional two-port power converters are often underutilized, especially in scenarios where their controllability is poorly aligned with the variable and often unpredictable nature of demand profiles. This is particularly critical on radial feeders, which are susceptible to significant voltage deviations under generation-demand mismatches [3]. To address this issue, the concept of enhanced soft-open-points (ESOPs) has emerged. These devices interconnect adjacent radial feeders and coordinate with nearby RESs or ESSs, thereby enabling grid-support functionalities such as peak shaving and facilitating greater penetration of low-carbon energy sources [4, 5].

Simultaneously, the proliferation of dc-based systems—such as ESSs and electric vehicle (EV) chargers—has led to an increased number of conversion stages, which adversely impacts system cost, volume, and efficiency. Nevertheless, the widespread availability of energy sources and sinks opens up opportunities for local energy aggregation and sharing. In high converter-density environments, such as residential or commercial buildings, there is significant potential for more streamlined energy integration, resulting in improved overall energy utilization.

Multiport power converters (MPCs), shown in Fig. 1, offer a promising solution by consolidating multiple energy interfaces—ac and dc—into a single, unified conversion platform [6]. With high controllability and flexibility, MPCs enable efficient energy exchange among various ports, while meeting local constraints such as voltage quality and power balancing. Their inherent capability to reduce the number of required conversion stages relative to conventional multi-terminal ac or dc solutions positions them as attractive candidates for achieving higher power density and cost-effectiveness in modern distribution networks [7].

MPCs are highly versatile, offering configurable port characteristics (ac or dc) and scalable port count, which makes them ideal for acting as centralized energy hubs. These hubs can seamlessly connect multiple feeders, substations, and distributed energy resources. Compared to systems composed of several dedicated two-port converters, MPCs reduce the overall footprint, cost, and complexity, while delivering enhanced power density and

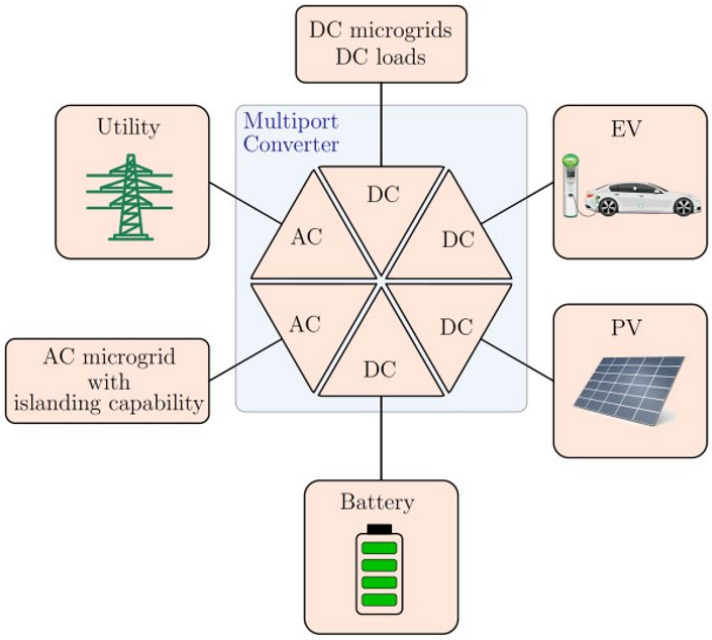


Figure 1: Represntation of a Multiport converter interfacing various sources, loads and storages.

integration flexibility.

Another notable advantage of MPCs is their advanced control, communication, and computational capabilities. These features enable decentralized operation, allowing local decision-making without relying solely on centralized grid management. This distributed intelligence fosters faster, more coordinated responses to dynamic grid events, thereby improving resilience and stability [8, 9].

On a broader level, MPCs are capable of performing localized grid-support functions—such as voltage regulation, frequency support, and continuity of service—while also contributing to system-wide objectives like efficiency optimization, load balancing, and congestion management. Their flexibility enables them to act as both local controllers and system-level optimizers [10]. Furthermore, future advancements in MPC control will leverage adaptive, data-driven algorithms capable of evolving in response to real-time grid conditions. These adaptive strategies will enhance security, power quality, and dynamic robustness.

The primary objective of WP3 is to investigate and facilitate the deployment of MPCs in low-voltage (LV) distribution networks, addressing both household and broader distribution-level scenarios. Key research directions include the development of compact, high-efficiency circuit topologies capable of interfacing multiple dc ports with single-phase or three-phase ac grids. This will reduce the number of conversion stages, minimize passive component size, and improve overall converter power density.

In parallel, WP3 addresses key control and modulation challenges, including the real-

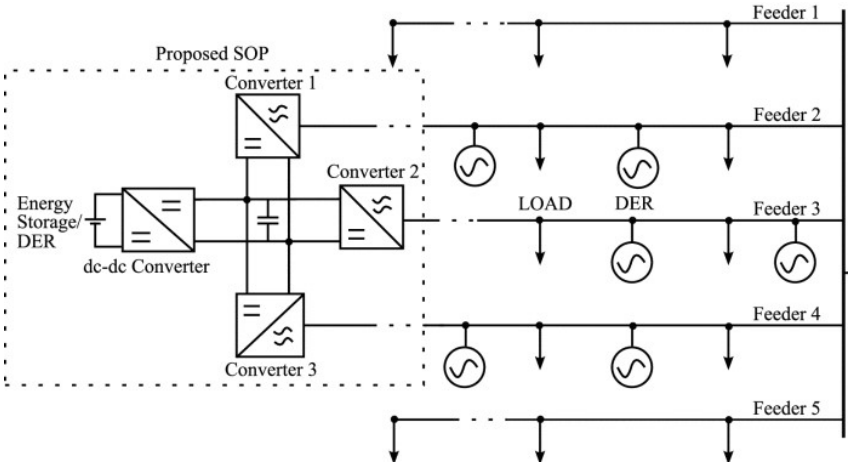


Figure 2: Multiport converter for distribution level scenario.

ization of Zero-Voltage Switching (ZVS) across varying operating conditions. Advanced control methods—such as oversampling techniques and digital hysteresis modulation—will be employed to enhance current and voltage regulation, while preserving passivity and ensuring high control bandwidth across all ports. These innovations are essential to mitigate dynamic instabilities and oscillatory behavior in increasingly complex and flexible future grids.

2.2 Scope of WP3 Research Activities

In distribution level scenario where DNs have a significant penetration of renewable sources such as solar PV and wind power plants, along with various industrial loads, electric vehicle charging stations, and energy storage units, power electronics play a vital role. They facilitate the integration of renewables and energy storage systems, optimize the use of the distribution network, and enable the connection of various loads at different voltage levels, both AC and DC as presented in Fig. 2. Several power-electronic solutions have been discussed in the literature for enhancing capacity, improving flexibility, and enhancing controllability in distribution grids. These solutions include ESOP, smart transformers, and multiport converters. Additionally, there is a growing interest in introducing multiport converters in residential areas to accommodate future connections of EVs and distributed renewable generation. For example, a multiport converter has the capability to interconnect two low-voltage (LV) lines in a region to improve the balance of loads, voltages, and renewable capacity.

For distribution-level MPCs, back-to-back voltage source converters (VSCs) have demonstrated superior performance at high power levels and have been widely reported in various industrial projects. Therefore, the topology evaluation of distribution-level MPCs is considered well-covered in the literature [11, 12]. Additionally, as shown for two-port VSCs,

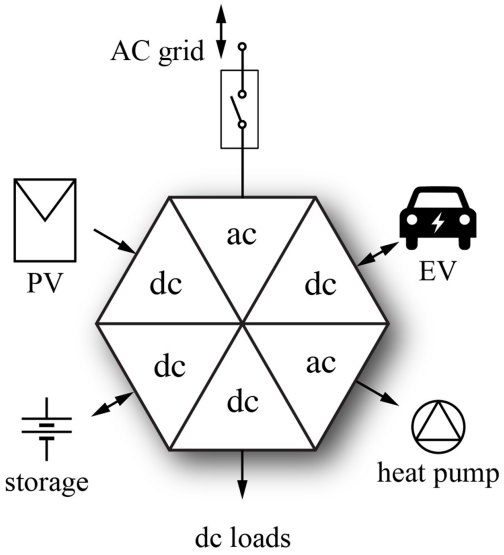


Figure 3: Multiport converter for residential level scenario.

three-level and multi-level VSCs can potentially improve performance compared to two-level VSCs, and these findings can be readily extended to back-to-back VSCs [13, 14].

In household/residential settings, MPCs can play a pivotal role in linking local RESs and ESSs with the broader distribution grid as displayed in Fig. 3. Additionally, multiple ports of the converter can be designed to support local energy storage systems and electric vehicles. Implementing MPCs in household installations offers substantial advantages, including enhanced system efficiency and reduced integration costs for renewable energy, EVs, and energy storage compared to traditional methods. This approach not only optimizes energy management at the household level but also contributes to the overall stability and efficiency of the distribution network, paving the way for more resilient and cost-effective energy solutions.

For household/residential scenario, The primary technical and scientific objectives are threefold: First, it aims to provide a detailed assessment and evaluation of MPCs in low-voltage (LV) applications compared to multiple converters. This will involve a comprehensive analysis of losses, volume, and optimization of semiconductor devices and passive elements, considering factors such as switching frequency and wide bandgap device technologies. Second, the project seeks to propose novel MPC topologies to overcome existing limitations, such as reliance on DC-link or magnetic coupling, restrictions on power exchange, and the presence of circulating currents. These novel topologies will aim for single-stage power conversion, enhanced efficiency, power density, and bidirectional power flow at all ports. Third, the project will focus on ensuring reliable and high-performance control of MPCs through advanced controllers, oversampling, and digital hysteresis modulation,

addressing dynamic interactions and minimizing disturbances with other power electronics converters in distribution grids.

2.3 Interrelations with WP3 Previous Deliverable (D3.1)

Deliverable 3.1 [1] of the iPLUG project provided the initial foundations for WP3, identifying the core challenges associated with soft open point (SOP) converters in LV networks, and introducing a passivity-oriented control framework to ensure robust stability. Key outcomes included the proposal of novel single-stage, non-isolated multiport converter topologies for residential applications and the demonstration of improved dynamic performance via a non-linear control law applied to the Y-converter.

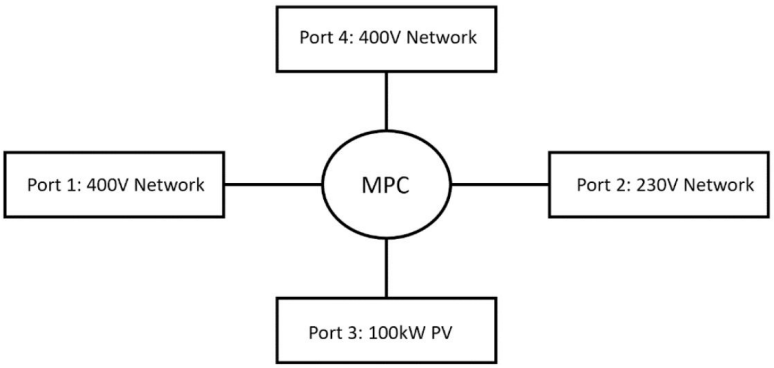
Building directly on those results, Deliverable D3.2 shifts focus from topology and control design to hands-on experimental validation. The laboratory prototypes developed here embody the single-stage MPC architectures introduced in D3.1 [1], and are tested under both steady-state and dynamic operating conditions that emulate real-world grid-interfacing and energy-management scenarios.

Furthermore, D3.2 extends the scope of evaluation by incorporating a multi-objective optimization framework, targeting simultaneously high conversion efficiency and elevated power density—two metrics that are critical for compact, cost-effective LV power conversion. Comparative studies against cascaded two-port converter arrangements demonstrate that the MPCs deliver superior system-level efficiency and reduced component count under renewable-generation mission profiles. Finally, the non-linear control strategy first developed for the Y-converter in D3.1 [1] has been refined and generalized to the broader MPC scenario.

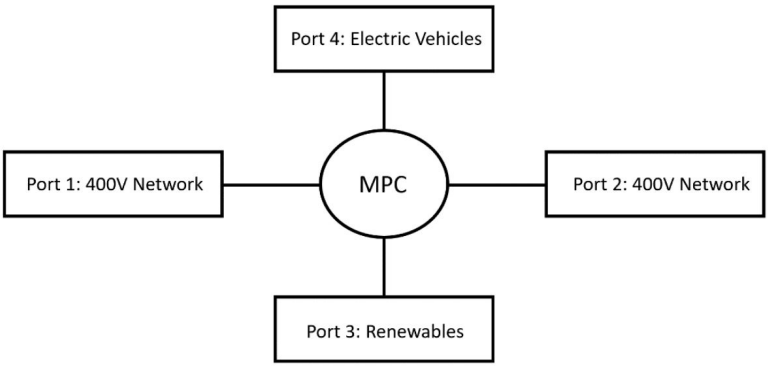
2.4 Interrelations with Other WPs in the iPlug Project

The activities of WP3 are organized to align with the outcomes of WP1, ensuring compliance with grid codes and standards, considering the defined KPIs for evaluating different converters, and adopting the case studies presented in WP1. The following case studies, shown in Fig. 4, have been considered in WP3 activities: Case Study 2.2 for interconnection of LV feeders, Case Study 2.4 for LV residential areas, and Case Study 4 for smart home installations.

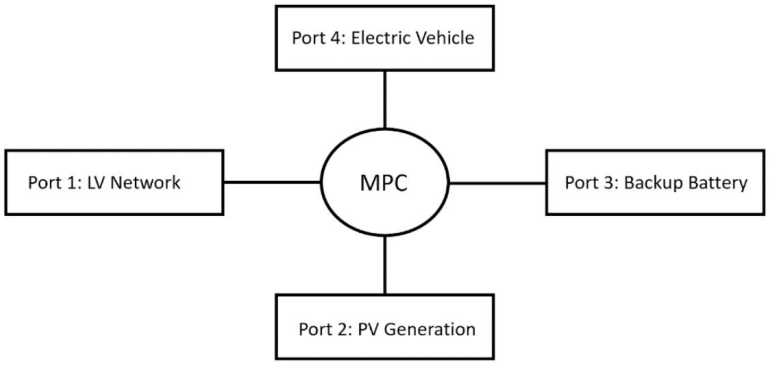
Considering the interrelation with WP2, the proposed control techniques for FRT and impedance passivity can be extended to the medium-voltage case studies addressed in WP2. Additionally, the evaluation studies presented in WP3 can provide valuable insights for topology evaluation and ranking in WP2. Moreover, both WP2 and WP3 shared the same approach of rapid prototyping using Imperix modules and controllers for prototype development and experimental verification. For WP4, the proposed converters in WP3 and



(a) Case study 2.2



(b) Case study 2.4



(c) Case study 4

Figure 4: WP1 case studies utilized in WP3 activities.

the impedance passivity approach can be utilized in the grid-interaction studies undertaken in WP4.

2.5 Summary of Contributions in This Deliverable

2.5.1 Experimental Prototype Development for the Proposed Multiport Converters

A rapid-prototyping setup is employed to enable flexible experimental testing of the proposed multiport converters under both steady-state and dynamic conditions.

The experimental prototype integrates two distinct types of half-bridge modules, each selected or custom-designed to meet the specific electrical and functional requirements of the respective stages in the multiport converter.

Six commercial Imperix PEB8024 half-bridge power modules are used for the boost stages. These modules incorporate C2M0080120D SiC MOSFETs, providing robust switching performance along with integrated protection features, which are advantageous for rapid development. However, the C2M0080120D devices exhibit a relatively high on-state resistance of $80\,\mathrm{m\Omega}$, contributing to elevated conduction losses, particularly under high current operation. Additionally, each Imperix module includes a sizable built-in dc-link capacitor of $235\,\mu\mathrm{F}$, which, while beneficial for stabilizing the dc voltage, results in significant reactive power consumption when interfacing with the ac grid.

To meet the specific requirements of the buck stages—especially those connected to the ac grid—three custom-designed half-bridge modules are developed. These modules utilize UF4SC120023K4S SiC MOSFETs, which offer a significantly lower on-state resistance of $23\,\mathrm{m\Omega}$, thus reducing conduction losses under high current conditions. Moreover, the custom modules feature a modular and adjustable dc-link capacitance, configurable between $3.5\,\mu\mathrm{F}$ and $20\,\mu\mathrm{F}$, providing greater flexibility and improved compatibility with grid-connected applications.

This deliverable presents a detailed description of the main building blocks of the prototype, including the semiconductor devices, control architecture, power supplies, power measurement instruments, and related hardware components.

2.5.2 Experimental Validation of the Proposed Symmetric and Asymmetric Multiport Y-converters

A detailed experimental validation of both the symmetric and asymmetric variants of the proposed multiport Y-converter is presented in this deliverable. The developed hardware prototypes have been extensively tested under a variety of operating scenarios to verify the theoretical analysis, assess dynamic behavior, and evaluate performance metrics such as current sharing, voltage regulation, power conversion efficiency, and grid current quality.

The experimental setup replicates real-world conditions through the integration of bidirectional ac and dc programmable power supplies, real-time control platforms, and precision measurement instruments. Both converters were subjected to steady-state and dynamic load conditions to capture their transient response, stability margins, and their ability to handle power flow in both directions across ports. Emphasis was placed on validating the correct operation during different load distributions among the dc ports and across multiple operating modes, such as charging, discharging, and simultaneous bidirectional power exchange.

Waveforms captured using high-speed oscilloscopes and real-time data acquisition systems confirm that the converters maintain balanced three-phase grid currents with low total harmonic distortion (THD), even during fast transients. In the symmetric configuration, the results demonstrate uniform power distribution and consistent port behavior due to structural uniformity. In contrast, the asymmetric configuration reveals its capability to manage differential power flows efficiently, thanks to its flexible control strategy and hardware asymmetry tailored for application-specific requirements.

The performance of both prototypes was benchmarked in terms of efficiency across a wide range of operating powers. Using calibrated power meters and synchronized current and voltage measurements, efficiency curves were derived and evaluated.

2.5.3 Performance Evaluation of Multiport Y-Converters using Renewable Source Mission Profile

To further highlight the potential of MPCs, the design and optimization of converter topologies for interconnecting 400 V dc MGs with the European low-voltage ac grid is conducted. The Y-converter topology is investigated, offering single-stage power conversion and bidirectional buck–boost capability. Two design approaches are evaluated: employing separate two-port Y-converters (2Y) and utilizing a single, integrated multiport Y-converter. A Pareto optimization framework is applied to explore trade-offs between efficiency and power density, based on detailed analysis of component losses, volume, and design constraints. Results show that both approaches achieve high efficiency and power density, with the MPC exhibiting superior average efficiency for dc power transfer by avoiding additional losses introduced by the intermediate ac stage present in the 2Y configuration. These findings demonstrate the strong potential of MPCs as compact and efficient interfaces for future dc MGs integration with the ac grid.

2.5.4 Proposing Nonlinear Control of Y-Converters for Grid Integration of 400 V DC Microgrids

A loss-free resistor hysteresis controller is proposed for the Y-converter as an alternative approach to the conventional linear controllers. The motivation for employing loss-free resistor hysteresis controller over traditional linear controllers lies in its ability to significantly enhance the dynamic performance of power converters. Linear controllers, while widely used, often struggle with rapid transient responses and maintaining stability across a wide range of operating conditions due to their inherent reliance on fixed gain settings and limited bandwidth. In contrast, loss-free resistor hysteresis control dynamically adjusts the switching actions based on real-time system conditions, allowing for precise control of current and voltage with minimal delay. This method also improves response times to transient events and maintains stable operation without the need for complex compensation networks. Additionally, hysteresis control inherently adapts to variations in load and supply conditions, providing a robust solution that enhances overall system reliability. The proposed controller is initially proposed for two-port converter and then extended to multiport converter scenario.

2.6 List of Publications

A set of relevant publications has been realized within WP3, as follows:

- M. D. Hernàndez, O. Esquius Mas, M. C. Mañe, E. Prieto Araujo and O. G. Bellmunt, ”Fault Ride Through Control of Multiport Converter for Distribution Grids,” 2022 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe), Novi Sad, Serbia, 2022, pp. 1-5, doi: 10.1109/ISGT-Europe54678.2022.9960596.
- A. Y. Farag, D. Biadene, P. Mattavelli and T. Younis, ”Three-phase Four-wire Bidirectional Y-converter for an Enhanced Interface between the AC Grid and the Unipolar DC Microgrid,” 2023 8th IEEE Workshop on the Electronic Grid (eGRID), Karlsruhe, Germany, 2023, pp. 1-6, doi: 10.1109/eGrid58358.2023.10380894.
- R. Cvetanovic, I. Petric, P. Mattavelli and S. Buso, ”MIMO Analysis of Port-Coupling Induced Destabilization of Interlinking DC-DC Converters,” 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 2806-2813, doi: 10.1109/APEC48139.2024.10509432.
- K. A. A. Mohammed, P. Mattavelli, T. Caldognetto, D. Biadene and P. Magnone ”Analysis of Low Voltage Ride Through Capability in Multiport Converters for Soft-Open Point Applications,” ELECTRIMACS 2024, Castello de la Plana, Spain.

- A. Y. Farag, D. Biadene, T. Caldognetto and P. Mattavelli, ”Enhancing DC Microgrids Integration with Three-Phase AC Grids Using Multiport Converters,” 2024 Power Electronics, Machines and Drives 13th International Conference PEMD 2024, Nottingham, United Kingdom.
- A. Y. Farag, D. Biadene, P. Mattavelli and T. Younis, ”Three-Phase Four-Wire Step-Down Modular Converter for an Enhanced Interlinking in Low-Voltage Hybrid AC/DC Microgrids,” in IEEE Open Journal of Power Electronics, vol. 5, pp. 634-647, 2024, doi: 10.1109/OJPEL.2024.3394548.
- A. Y. Farag, D. Biadene, T. Caldognetto and P. Mattavelli, ”Multiport Y-Converter for Three-Phase AC Grid Integration with DC Systems,” 2024 IEEE 15th International Symposium on Power Electronics for Distributed Generation Systems PEDG 2024, Luxembourg, 2024.
- A. Y. Farag, D. Biadene, T. Caldognetto and P. Mattavelli, ”Asymmetric Multiport Y-Converter for Three-Phase AC Grid Integration with DC Microgrids,” 2024 Energy Conversion Congress & Expo Europe (ECCE Europe).
- R. Cvetanović, I. Z. Petrić, P. Mattavelli and S. Buso, ”On the Applicability of SISO and MIMO Impedance-Based Stability Assessment of DC–DC Interlinking Converters,” in IEEE Transactions on Power Electronics, vol. 39, no. 9, pp. 10768-10780, Sept. 2024, doi: 10.1109/TPEL.2024.3403236.
- R. Cvetanović, I. Z. Petrić, P. Mattavelli and S. Buso, ”All-Port MIMO Admittance Passivity for Robust Stability of DC-DC Interlinking Converters,” in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2024.3430560.
- A. Y. Farag, D. Biadene, T. Caldognetto and P. Mattavelli, ”Single-Stage Non-Isolated Multiport Y-Converter for Interlinking 400 V DC Microgrids With the Three-Phase AC Grid,” in IEEE Open Journal of Power Electronics, vol. 5, pp. 1432-1445, 2024, doi: 10.1109/OJPEL.2024.3462773.
- K. A. A. Mohammed, A. Y. Farag, D. Biadene, T. Caldognetto and P. Mattavelli, ”Performance Evaluation of Multiport Y-Converters using Renewable Source Mission Profile,” IEEE 7th International Conference on DC Microgrids ICDCM 2025 **(To be presented)**.
- M.B. Debbat, A. Y. Farag, P. Mattavelli, JL. Domínguez-García ”Nonlinear Control of the Four-Wire Y-Converter for Grid Integration of 400 V DC Microgrids,” IEEE 7th International Conference on DC Microgrids ICDCM 2025. **(To be presented)**.
- K. A. A. Mohammed, A. Y. Farag, D. Biadene, T. Caldognetto, P. Magnone and P. Mattavelli, ”Isolated Y-Connected Multiport Converter for Interconnecting DC Systems

with the AC Grid," In IEEE Energy Conversion Conference and Expo ECCE-2025. **(To be presented)**.

- A. Y. Farag, D. Biadene, T. Caldognetto, P. Magnone and P. Mattavelli, "Modified Discontinuous Modulation for Mitigating Distortions at Phase Clamping in Y-Converter," In IEEE Energy Conversion Conference and Expo ECCE-2025. **(To be presented)**.
- A. Y. Farag, D. Biadene, T. Caldognetto, P. Magnone and P. Mattavelli, "Low-Frequency Voltage-Ripple Minimization of Asymmetric Multiport Y-Converter," In IEEE Transactions on Power Electronics. **(under review)**.
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3 Experimental Verification of the Multiport Y-Converter

This section briefly reviews the fundamental operation and analysis of the proposed symmetric multiport Y-converter, with the primary focus on prototype development and experimental validation. A more comprehensive analysis and evaluation of the multiport Y-converter can be found in D3.1 [1].

3.1 Brief Analysis and Background

3.1.1 Derivation and Operation Principle

The proposed multiport converter topology is derived from the Y-converter, as depicted in Fig. 5a, transforming it from a two-port configuration into a multi-port structure capable of connecting multiple dc ports to a three-phase ac grid, as illustrated in Fig. 5b. Initially, the two-port Y-converter comprised three four-switch buck-boost modules [15, 16]. Alternatively, in the proposed converter, each module is expanded into a six-switch dc-dc converter. Considering the structure of a three-port converter, the upgraded design includes a shared buck half-bridge and two boost half-bridges, establishing connections to the dc ports. Notably, the configuration is potentially adaptable to additional dc ports by incorporating one boost converter into each module for every extra dc port, thus maintaining scalability.

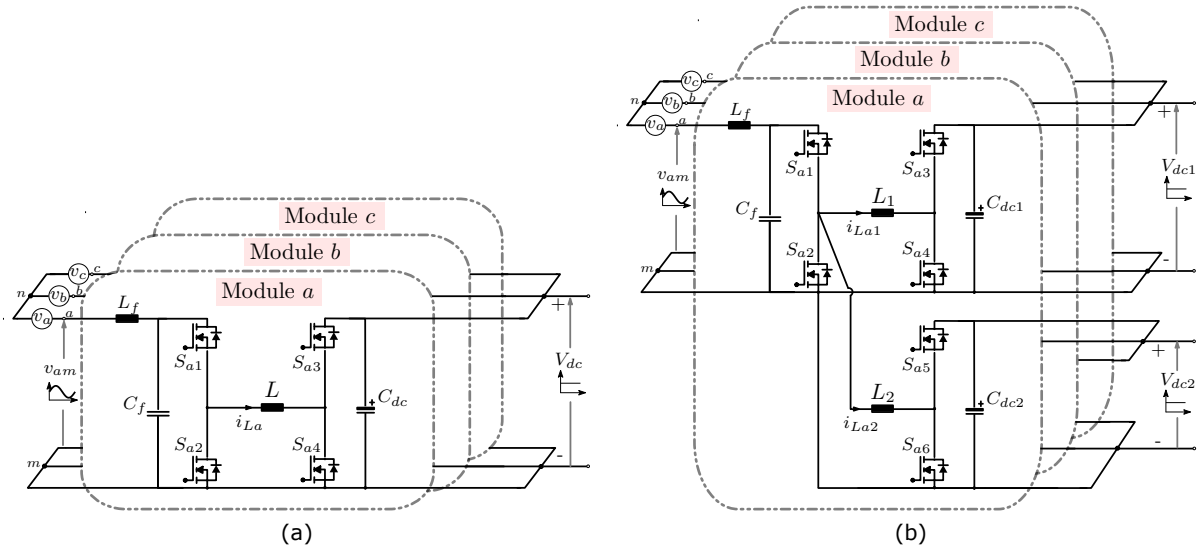


Figure 5: A schematic of two-port and multiport Y-converters in a modular form: (a) Two-port Y-converter; (b) The symmetric Multiport Y-converter.

Similar to the two-port Y-converter, the three modified modules are interconnected at a central point denoted as m, serving as the neutral point for the Y-connection of the modules. Since each module functions as a dc-dc converter, maintaining a non-negative voltage on the ac side of the module ($v_{\{a,b,c\}m} \geq 0$V) is crucial. To achieve this, an offset voltage is

required between the grid's neutral point n and m. A constant offset voltage (V_{off}) is then applied, which must exceed the peak value of the ac grid phase voltage ($\hat{V}_m$). The ac-side voltages v_{am}, v_{bm}, and v_{cm} can be expressed as follows:

$$v_{xm}(t) = v_x(t) + V_{off} = \hat{V}_m \sin(\omega t + \theta_x) + V_{off} \tag{1}$$

where v_x, with $x = (a, b, c)$, represents the ac grid phase voltages, ω denotes the ac grid frequency in rad/s, and θ_x signifies the respective phase angles of v_x.

Since V_{off} also represents the common-mode voltage (CMV) of the converter, the fixed CMV is an additional advantage of the proposed topology. While CMV can pose a threat to overall system performance by inducing leakage current through parasitic capacitances to ground and causing electromagnetic interference (EMI) in the high-frequency range [17], the fixed CMV in the proposed topology minimizes these issues as the leakage current flowing through parasitic capacitances is significantly reduced.

The analysis of the converter is presented by considering a single module (module a), as depicted in Fig. 6, and it similarly applies to the other modules as well. This module consists of the two inductors L_1 and L_2 along with three half-bridges: one on the ac side, labeled as Bu_a, and the others on the dc sides, labeled as Bo_{a1} and Bo_{a2}. Although the main focus of this article is on interfacing 400 V dc systems, the subsequent analysis is generalized for arbitrary values of V_{dc1} and V_{dc2}. Additionally, it is assumed that at least one of the dc ports' voltage is lower than the peak of the ac side voltage ($\hat{V}_m + V_{off}$), and V_{dc1} is lower than V_{dc2}. Based on these assumptions, the Bu_a and Bo_{a1} half-bridges are under control, ensuring that only one of them is modulated at any given moment, while the other remains clamped based on the values of v_{am} and V_{dc1}, whereas Bo_{a2} will be modulated continuously.

3.1.2 Analysis and Fundamental Relations

3.1.2.1 Buck Mode When v_{am} exceeds V_{dc1}, module a operates in buck mode. In this mode, the Bu_a half-bridge switches, while the Bo_{a1} half-bridge is clamped with S_{a3} on and S_{a4} off, as illustrated in Fig. 7a. Simultaneously, the Bo_{a2} half-bridge operates with a fixed duty cycle, depending on the ratio between V_{dc1} and V_{dc2}. The duty cycles of S_{a1} and S_{a5}, denoted as d_{Bu_a} and $d_{Bo_{a2}}$, respectively, can be calculated using the following equations:

$$d_{Bu_a}(t) = \frac{V_{dc1}}{v_{am}(t)} = \frac{V_{dc1}}{\hat{V}_m \sin(\omega t) + V_{off}} \tag{2}$$

$$d_{Bo_{a2}} = \frac{V_{dc1}}{V_{dc2}} \tag{3}$$

The ac grid current of phase a, denoted as i_a, is assumed to be pure sinusoidal and in

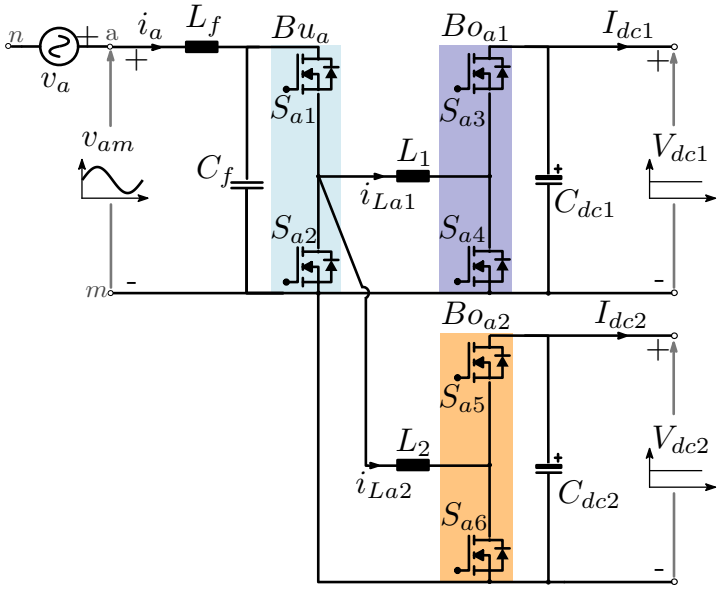


Figure 6: Module a of the proposed converter.

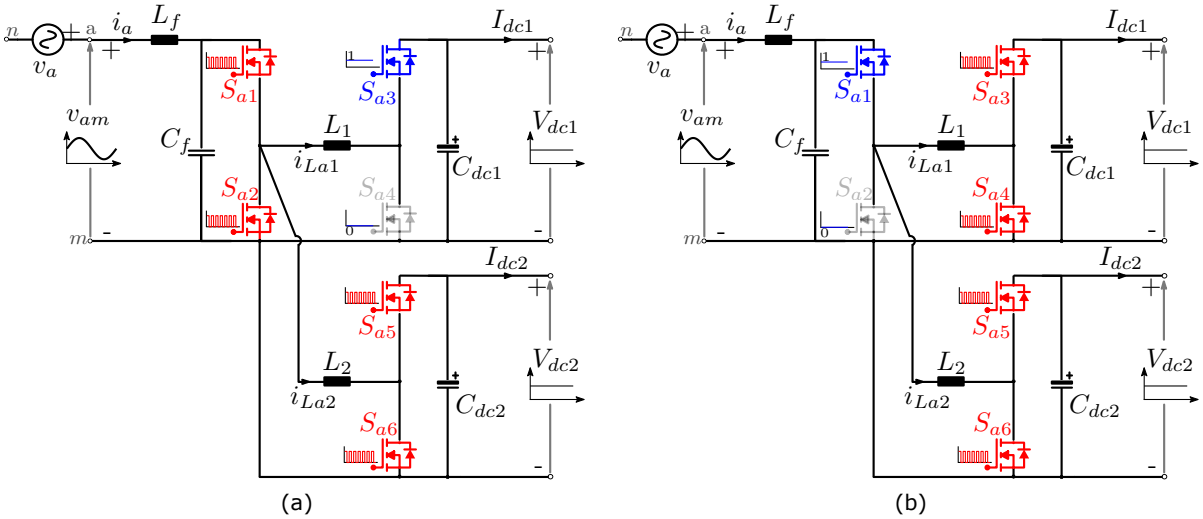


Figure 7: Operation modes of one module of the proposed converter: (a) Buck mode when $v_{am} > V_{dc1}$; (b) Boost mode when $v_{am} < V_{dc1}$

phase with its corresponding phase voltage v_a and then can be calculated as follows:

$$\begin{aligned} i_a(t) &= \hat{I}_m \sin(\omega t) = (\hat{I}_{m1} + \hat{I}_{m2}) \sin(\omega t) \\ &= \left(\frac{2P_{dc1}}{3\hat{V}_m} + \frac{2P_{dc2}}{3\hat{V}_m} \right) \sin(\omega t) \end{aligned} \tag{4}$$

where P_{dc1} and P_{dc2} represent the power delivered to dc ports 1 and 2, respectively, while $\hat{I}_m$ denotes the peak phase current. Additionally, $\hat{I}_{m1}$ and $\hat{I}_{m2}$ signify the equivalent reference peak phase current solely due to the power of dc MG#1 and #2, respectively.

The summation of average inductor currents (i.e., $i_{La1,av}$ + $i_{La2,av}$), denoted as $i_{La,av}$, can be derived by applying Kirchhoff's current law (KCL) at the ac input of the module, as follows:

$$i_{La,av}(t) = i_{La1,av}(t) + i_{La2,av}(t) = \frac{i_a(t) - i_{Cf,a}(t)}{d_{Bu_a}(t)} \tag{5}$$

where $i_{Cf,a}$ represents the current through the input capacitor C_f. By neglecting $i_{Cf,a}$, the equation can be simplified as follows:

$$i_{La,av}(t) = \frac{i_a(t)}{d_{Bu_a}(t)} = \frac{\hat{I}_m \sin(\omega t)}{d_{Bu_a}(t)} \tag{6}$$

Using (4) and (6) , $i_{la1,av}$ and $i_{la2,av}$ can be determined as follows:

$$\begin{aligned} i_{La1,av}(t) &= \frac{\hat{I}_{m1} \sin(\omega t)}{d_{Bu_a}} \\ i_{La2,av}(t) &= \frac{\hat{I}_{m2} \sin(\omega t)}{d_{Bu_a}} \end{aligned} \tag{7}$$

3.1.2.2 Boost Mode The second mode of operation occurs when v_{am} falls below V_{dc1}. In this mode, module a operates in boost mode. In this mode, the Bo_{a1} half-bridge switches, while the Bu_a half-bridge is clamped with S_{a1} on and S_{a2} off, as depicted in Fig. 7b. Simultaneously, the Bo_{a2} half-bridge operates with a time-varying duty cycle. The duty cycles of S_{a3}, denoted as $d_{Bo_{a1}}$, and $d_{Bo_{a2}}$ can be calculated using the following equations:

$$d_{Bo_{a1}}(t) = \frac{v_{am}(t)}{V_{dc1}} \tag{8}$$

$$d_{Bo_{a2}}(t) = \frac{v_{am}(t)}{V_{dc2}} \tag{9}$$

Using (7) and given that $d_{Bu_a} = 1$ in this mode, $i_{La1,av}$ and $i_{La2,av}$ can be determined as:

$$\begin{aligned} i_{La1,av}(t) &= \hat{I}_{m1} \sin(\omega t) \\ i_{La2,av}(t) &= \hat{I}_{m2} \sin(\omega t) \end{aligned} \tag{10}$$

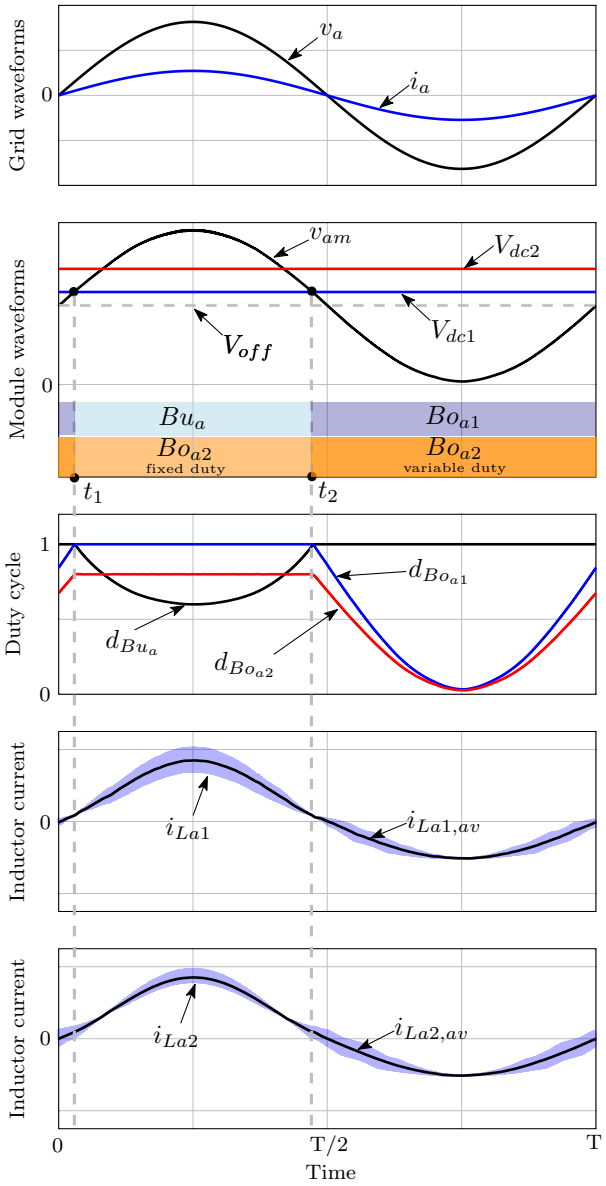


Figure 8: Key waveforms of module a of the proposed converter.

The key waveforms for module a of the proposed converter are plotted in Fig. 8. Additionally, the basic characteristic equations of the proposed converter are summarized in Table 1. These equations are applicable to any values of V_{dc1} and V_{dc2}, including the scenario presented in the analysis (where V_{dc1} is lower than V_{dc2}) and also when V_{dc1} is higher than V_{dc2}.

3.2 Description of the Experimental prototype

This section provides a detailed overview of the experimental prototype used to validate both the symmetric and asymmetric multiport Y-converters, highlighting the main components along with their key features and specifications. Fig. 9 shows the rapid-prototyping

Table 1: Summary of the basic equations of the proposed converter.

Parameter	Equation	Parameter	Equation
v_x	$\hat{V}_m \sin(\omega t + \theta_x)$	v_{xm}	$v_x + V_{off}$
d_{Bu_x}	$\frac{\min(v_{xm}, V_{dc1}, V_{dc2})}{v_{xm}}$	$d_{Bo_{x1}}$	$\frac{\min(v_{xm}, V_{dc1}, V_{dc2})}{V_{dc1}}$
$d_{Bo_{x2}}$	$\frac{\min(v_{xm}, V_{dc1}, V_{dc2})}{V_{dc2}}$	$i_{Lx,av}$	$\frac{\hat{I}_m \sin(\omega t + \theta_x)}{d_{Bu_x}}$
$i_{Lx1,av}$	$\frac{2P_{dc1} \sin(\omega t + \theta_x)}{3\hat{V}_m\, d_{Bu_x}}$	$i_{Lx2,av}$	$\frac{2P_{dc2} \sin(\omega t + \theta_x)}{3\hat{V}_m\, d_{Bu_x}}$

setup employed to facilitate flexible experimental testing of the proposed converters under both steady-state and dynamic conditions. While this approach enables quick verification of functionality and control performance, it does not yield optimized efficiency or power density; those optimization efforts are discussed later in this deliverable.

3.2.1 Semiconductor devices

The experimental prototype integrates two different types of half-bridge modules, each selected and designed to optimally fulfill the requirements of the respective stages in the multiport converter. The prototype consists of six commercial Imperix PEB8024 half-bridge power modules are employed. These modules utilize C2M0080120D SiC MOSFETs and the modules offer reliable switching performance and integrated protection features, making them well-suited for rapid prototyping and development. However, they come with certain limitations: the MOSFETs exhibit a relatively high on-state resistance of $80\,\mathrm{m\Omega}$, leading to increased conduction losses, particularly under high current conditions. Furthermore, each module includes a substantial built-in dc-link capacitance of $235\,\mu\mathrm{F}$, which, although beneficial for voltage dc voltage stabilization, when connected to ac grid it consumes a high reactive power.

To address the specific demands of the buck stages—particularly those interfacing with the ac grid—three custom half-bridge modules were designed. These modules are built around the UF4SC120023K4S SiC MOSFETs, which feature significantly lower on-state resistance ($23\,\mathrm{m\Omega}$). This characteristic is essential to reduce conduction losses during high-current operation, which is more critical on the ac side. In contrast to the Imperix modules, the custom boards incorporate a modular and adjustable dc-link capacitance, ranging from $3.5\,\mu\mathrm{F}$ to $20\,\mu\mathrm{F}$.

In addition to power stage considerations, both module types are equipped with suitable gate-driving and sensing circuitry. Isolated gate drivers with high dV/dt immunity ensure robust switching performance, while onboard sensing elements provide accurate current and voltage measurements for closed-loop control. The gate drivers are designed with adjustable dead-time settings, and each half bridge integrates current sensing of the half-

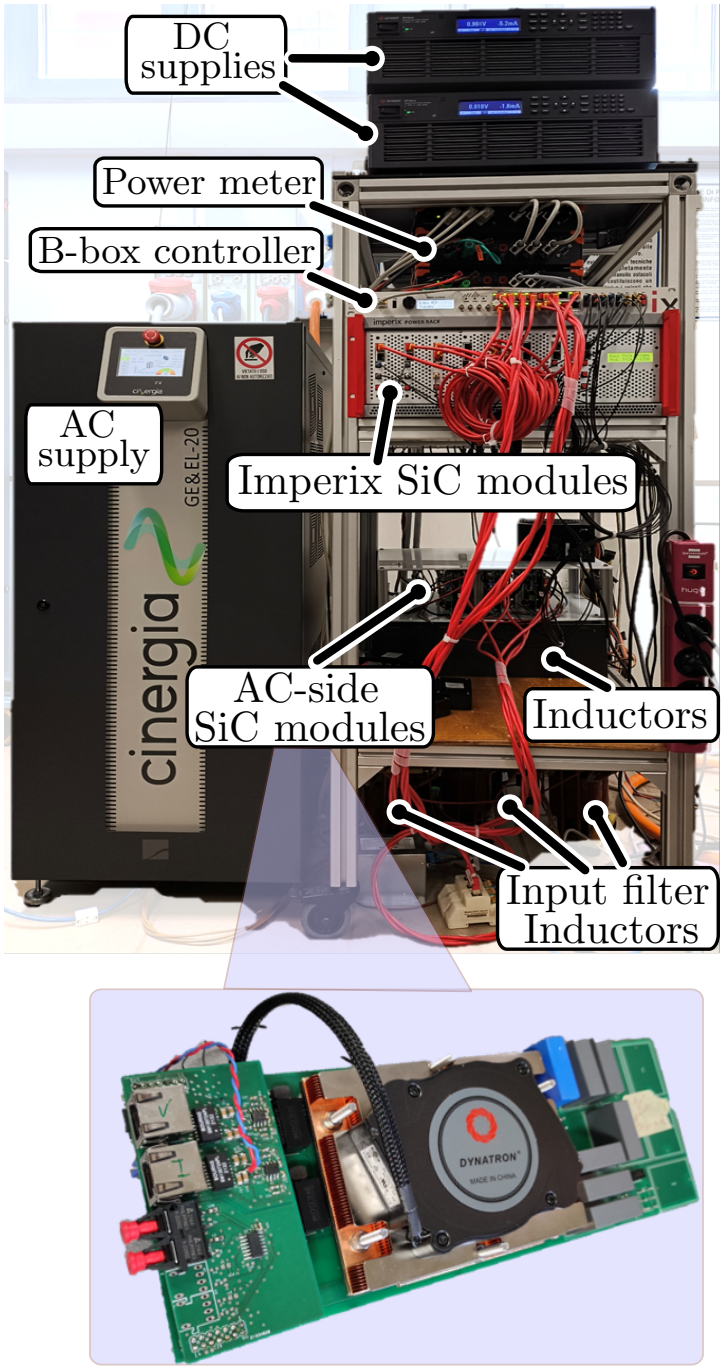


Figure 9: Picture of the experimental prototype of the proposed converter.

bridge's mid-point current and a voltage sensing for dc-link monitoring.

Overall, the combination of commercial modules for the boost stages and customized designs for the buck stages enables a flexible and efficient hardware platform. This hybrid approach supports comprehensive experimental validation of the proposed symmetric and asymmetric multiport Y-converters, capturing both steady-state and dynamic behavior under realistic grid-connected scenarios. It also establishes a foundation for future refinement toward a more power-dense and cost-optimized converter implementation.

3.2.2 Control architecture

The control architecture of the experimental prototype leverages two Imperix B-Box rapid control prototyping (RCP) controllers configured in a master-slave arrangement for the symmetric multiport Y-converter while a single B-Box is used for the asymmetric topology. This setup facilitates the management of complex multiport converter operations by distributing control tasks across the two units. The master controller oversees the primary control algorithms and coordinates the overall system behavior, while the slave controller handles auxiliary functions and specific control loops, ensuring synchronized operation across all converter ports.

Programming of the B-Box controllers is accomplished through MATLAB/Simulink, utilizing Imperix's Automated Code Generation (ACG) software development kit (SDK). This integration allows for seamless transition from simulation to real-time implementation, enabling rapid prototyping and iterative development of control strategies. The Simulink environment provides a user-friendly interface for designing control algorithms, which are then automatically converted into executable code for the B-Box controllers.

Real-time monitoring and debugging are facilitated by Imperix Cockpit, a comprehensive software tool designed for power electronics applications. Cockpit offers a suite of features including real-time visualization of control variables, parameter tuning without the need for code recompilation, and data logging capabilities. The software supports the creation of custom dashboards through its GUI Builder, allowing users to tailor the monitoring interface to specific application needs. Additionally, Cockpit enables the scheduling of transient events and the application of test scenarios, providing a robust platform for system validation and performance assessment.

3.2.3 Magnetic components

$330\,\mu$H inductors are employed for the main inductors L_1 and L_2, utilizing Fluxsan FS-301026-2 magnetic cores. Each inductor is wound with copper wire, resulting in a total resistance of $21\,\mathrm{m}\Omega$. Additionally, the grid-side filter inductor L_f is implemented using $1.2\,$mH inductors, constructed with ferrite cores and copper windings with a total resistance

of $30\,\mathrm{m}\Omega$. All inductors are designed to support a saturation current of $40\,\mathrm{A}$.

3.2.4 Power supplies

Bidirectional ac and dc power supplies are employed to emulate both the utility grid and the dc microgrid environments. The ac source is a Cinergia GE&EL-20, which provides a stable three-phase voltage waveform with adjustable amplitude and frequency to mimic grid conditions. On the dc side, two Keysight RP7962A units are used; each can operate either as a programmable dc source or as an electronic load. These dc supplies support both constant-voltage and constant-current modes, enabling tests under various load and source scenarios, including bidirectional power flow, transient response, and stability assessments.

3.2.5 Power Meter

To accurately evaluate the efficiency of the multiport converter prototype, the Dewesoft SIRIUS XHS high-speed data acquisition system is employed. This advanced system features HybridADC® technology, enabling both high-bandwidth transient recording and high-dynamic, alias-free acquisition. Each analog input channel supports sampling rates up to 15 MS/s with a 5 MHz bandwidth, allowing precise capture of rapid voltage and current transients across all ports of the multiport converter.

The SIRIUS XHS system offers flexible configuration options, with software-selectable modes per channel. This flexibility permits simultaneous acquisition of high-speed and high-dynamic signals, ensuring comprehensive measurement of the converter's performance under various operating conditions. The system's high galvanic isolation (up to CAT II 1000 V) between channels and to ground enhances measurement safety and accuracy, particularly in high-voltage environments.

Synchronization of multiple SIRIUS XHS units is achieved through the Precision Time Protocol (PTP v2), ensuring time alignment across all measurement channels. This capability is crucial for capturing synchronized voltage and current waveforms necessary for accurate power and efficiency calculations. The modular nature of the system allows for scalable expansion, accommodating additional measurement channels as required for complex multiport converter configurations.

Data acquisition and analysis are facilitated by the DewesoftX software, which provides real-time visualization, data logging, and post-processing capabilities. The software's power analysis module enables detailed evaluation of power parameters, including real-time calculation of efficiency metrics. This comprehensive suite of tools ensures that all aspects of the converter's performance are thoroughly assessed and documented.

Table 2: SiC devices and passive components utilized in the experimental prototype.

	Parameter	Symbol	Value
ac-side SiC MOSFET	Part number	UF4SC120023K4S	
	Voltage	V_{DS}	$1200\,\text{V}$
	On-state resistance	R_{DS}	$23\,\text{m}\Omega$
dc-side SiC MOSFET	Part number	C2M0080120D	
	Voltage	V_{DS}	$1200\,\text{V}$
	On-state resistance	R_{DS}	$80\,\text{m}\Omega$
Inductor parameters	Inductor	L_1, L_2	$330\,\mu\text{H}$
	Core part number	Fluxsan FS-301026-2	
	Inductor dc resistance	R_{Ldc}	$21\,\text{m}\Omega$
Input filter	Inductor	L_f	$1.2\,\text{mH}$
	Capacitor	C_f	$10\,\mu\text{F}$

3.2.6 Oscilloscope

To capture and analyze the experimental waveforms of the MPC prototype, a Tektronix MSO58 mixed-signal oscilloscope is employed. This advanced instrument offers eight inputs, each configurable as either an analog input or eight digital logic inputs, providing exceptional versatility for comprehensive signal monitoring. The MSO58 supports a maximum analog bandwidth of up to $2\,\text{GHz}$ and a real-time sampling rate of $6.25\,\text{Gsps}$ across all channels, ensuring high-fidelity acquisition of fast transient events and intricate waveform details.

In the experimental setup, the MSO58 is configured to simultaneously measure and display the following key electrical quantities: v_a, v_b, v_{am}, i_a, i_b, i_c, i_{La1}, and i_{La2}. The voltage v_c is not directly measured; instead, it is computed in real-time using the oscilloscope's internal math functions, leveraging the balanced nature of the imposed ac voltages, i.e., $v_c = -v_a - v_b$. This capability allows for efficient utilization of available channels while maintaining comprehensive voltage monitoring.

The specifications of the SiC devices and passive components utilized are summarized in Table 2.

3.3 Experimental Results

Experimental waveforms of the Y-MPC prototype are presented in Fig. 10 to showcase its performance under different operating conditions. For the presented operating points, V_{dc1} and V_{dc2} are set to $360\,\text{V}$ and $400\,\text{V}$, respectively, with the ac grid voltage set to its rated value. Additionally, P_{dc1} is fixed at $3\,\text{kW}$. The first operating point is displayed in Fig. 10a, where P_{dc2} equals $3\,\text{kW}$ so both MGs are absorbing power from the ac grid. As evident from the waveforms, the ac currents are sinusoidal and well-synchronized with the ac voltages,

resulting in a measured power factor equal to 0.99. The measured efficiency of the prototype at this operating point equal to 94.75%.

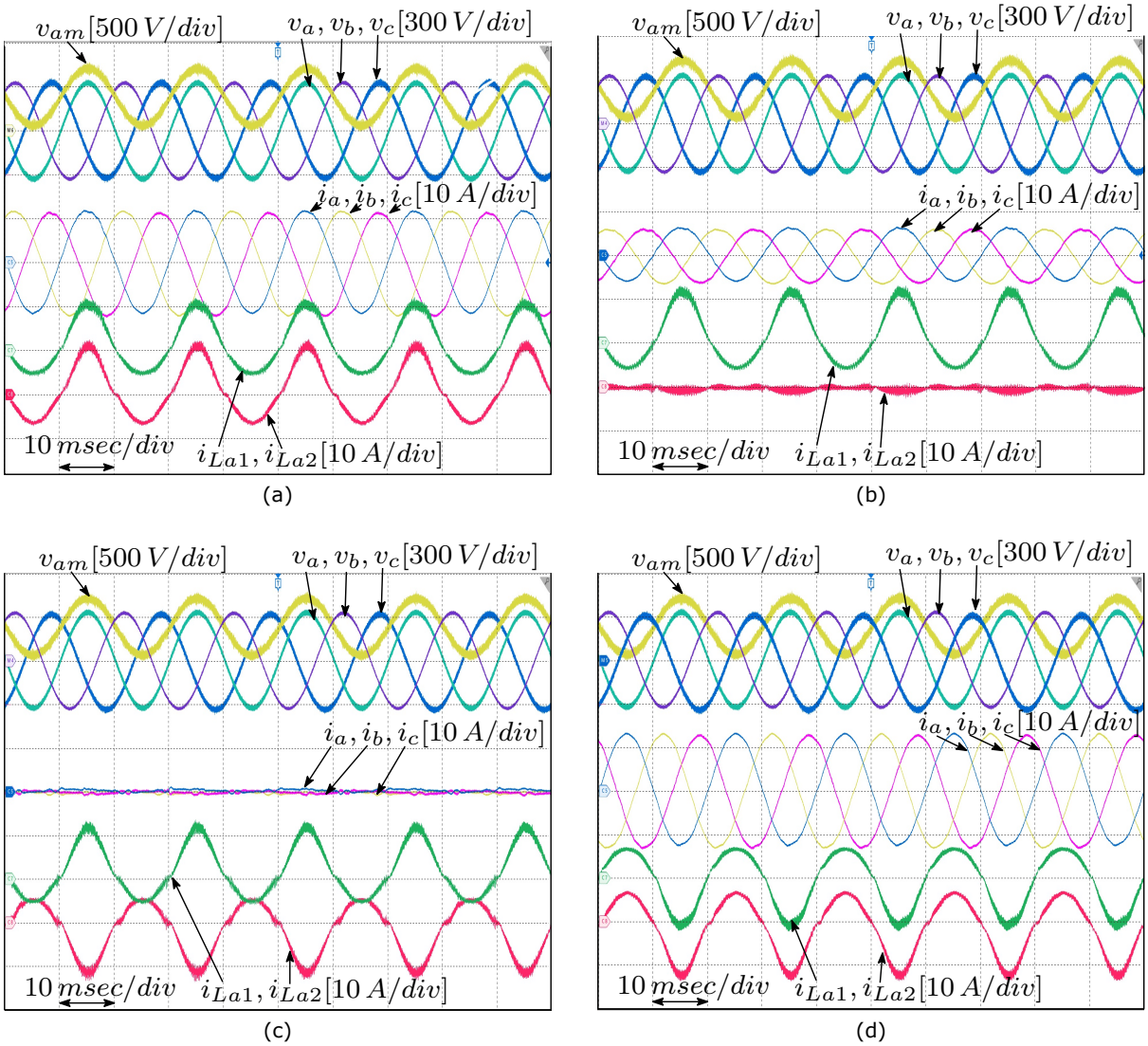


Figure 10: Experimental waveforms of the proposed converter with V_{dc1} and V_{dc2} are set to 360 V and 400 V under different values of P_{dc1} and P_{dc2}: (a) P_{dc1} and P_{dc2} both equal to 3 kW; (b) P_{dc1} and P_{dc2} equal to 3 kW and 0 kW, respectively; (c) P_{dc1} and P_{dc2} equal to 3 kW and -3 kW, respectively; and (d) P_{dc1} and P_{dc2} equal to -3 kW and -3 kW, respectively.

The second operating point is presented in Fig. 10b, where P_{dc2} is controlled to zero, representing the case when the power balance in dc MG#2 is attained only by its RESs, ESSs, and loads. Therefore, in this case, only MG#1 is absorbing power from the ac grid. To ensure zero power delivered to dc MG#2, i_{Lx2} is controlled to have an average low-frequency component set to zero. Therefore, in the presented waveforms, i_{La2} has only the high-frequency ripple component resulting in no power for dc MG#2. The waveform i_{La1} remains the same as in the first operating point due to the fixed value of P_{dc1}. The measured efficiency of the prototype at this operating point equal to 94.63%.

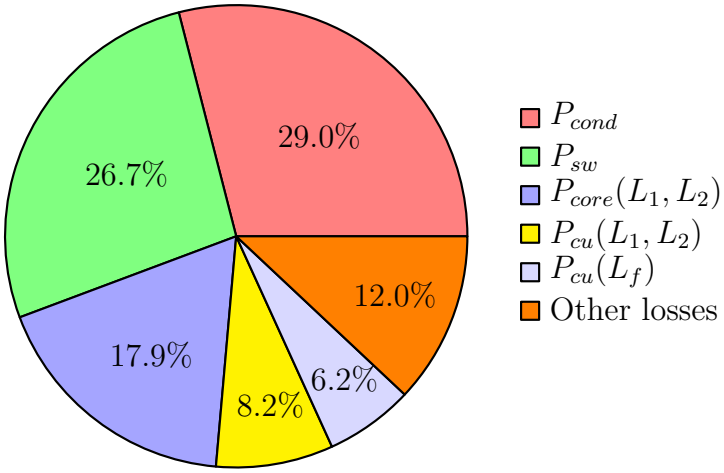


Figure 11: Calculated losses breakdown of the experimental prototype at P_{dc1} and P_{dc2} both equal to $3\,$kW.

In the third operating point, depicted in Fig. 10c, P_{dc2} is controlled to equal $-3\,$kW. This case represents when dc MG#2 has an excess of power generation, allowing it to meet the power demand of dc MG#1 directly through the Y-MPC, and hence no active power is drawn from the ac grid. In the presented waveforms, i_{La2} is inverted with respect to i_{La1} due to the different direction of power flow of the dc MGs. Additionally, as there is no active power drawn from the ac grid, the ac grid currents are minimized, and only the current due to the reactive power drawn by C_f flows. The measured efficiency of the prototype at this operating point equal to 95.71%.

In the last operating point, shown in Fig. 10d, both P_{dc1} and P_{dc2} are set to $-3\,$kW. This case represents when both dc MGs have a surplus power generation that is fed to the ac grid. In the presented waveforms, the ac grid currents are inverted with respect to their corresponding ac voltages, indicating the power flow direction to the ac grid. The measured efficiency of the prototype at this operating point equal to 94.73%.

The calculated power loss breakdown for the experimental prototype, with both P_{dc1} and P_{dc2} set to $3\,$kW, is presented in Fig. 11. The losses are categorized as follows: conduction and switching losses of semiconductor devices, denoted as P_{cond} and P_{sw}; core and copper losses of the main inductors, denoted as $P_{core}(L_1, L_2)$ and $P_{cu}(L_1, L_2)$; and copper losses of the input filter, denoted as $P_{cu}(L_f)$. The calculated losses indicate that total semiconductor losses represent 55.7% of the total losses, while the losses in the main inductors account for 26.1% of the total losses. The term ”other losses” includes losses not specifically calculated, such as those in the connections between modules, PCB losses, capacitor losses, etc., as well as the mismatch between the calculated and actual losses.

The transient behavior of the Y-MPC prototype is examined under various conditions. In Fig. 12a, the converter initially operates with P_{dc1} and P_{dc2} equal to $3\,$kW and $0.3\,$kW, respectively. P_{dc2} is then increased from $0.3\,$kW to $3\,$kW while keeping P_{dc1} constant. In

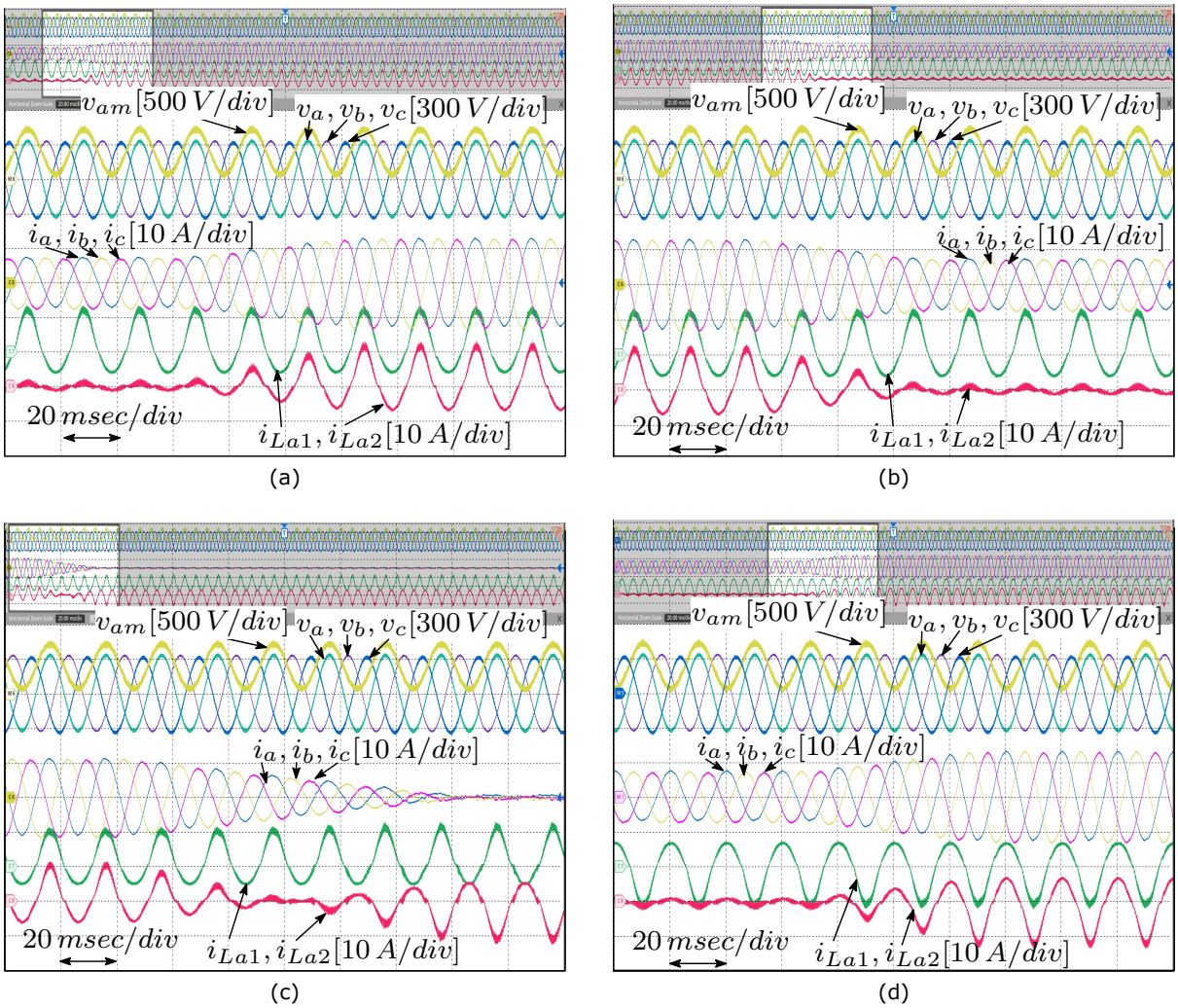


Figure 12: Experimental waveforms illustrating the transient behavior of the experimental prototype: (a) P_{dc1} equal to $3\,$kW and P_{dc2} increased from $0.3\,$kW to $3\,$kW; (b) P_{dc1} equal to $3\,$kW and P_{dc2} decreased from $3\,$kW to $0.3\,$kW; (c) P_{dc1} equal to $3\,$kW and P_{dc2} changed from $3\,$kW to $-3\,$kW; (d) P_{dc1} equal to $-3\,$kW and P_{dc2} changed from $-0.3\,$kW to $-3\,$kW.

Fig. 12b, P_{dc2} is decreased from $3\,$kW to $0.3\,$kW with P_{dc1} kept constant at $3\,$kW. In Fig. 12c, P_{dc2} is changed from $3\,$kW to $-3\,$kW with P_{dc1} kept constant at $3\,$kW, causing P_{ac} to drop from $6\,$kW to $0\,$kW. In Fig. 12d, P_{dc2} is changed from $-0.3\,$kW to $-3\,$kW with P_{dc1} kept constant at $-3\,$kW. The experimental results illustrate the change in i_{La2} to deliver the required P_{dc2}, while i_{La1} remains unaffected by the change in P_{dc2}, validating the power decoupling feature of the proposed converter and its ability to regulate the power flow to the dc MG#2 without causing a disturbance to the power flow of dc MG#1.

4 Experimental Verification of the Asymmetric Multiport Y-Converter

This section provides a comprehensive analysis of the asymmetric multiport Y-converter, addressing its various operating modes and highlighting key challenges associated with the topology, such as ac grid current balancing and minimization of low-frequency voltage ripple. In addition, an extensive experimental validation of the converter is presented to demonstrate its performance under realistic operating conditions.

4.1 Principle of Operation and Analysis

The proposed converter builds upon the Y-converter [15], transforming it from a two-port configuration into a multiport converter that interlinks multiple dc systems with the three-phase ac grid. As shown in Fig. 13a, the original two-port Y-converter consists of three four-switch buck-boost modules. To extend it into a multiport converter, the four-switch buck-boost converter is extended into a six-switch buck-boost converter, featuring a shared buck half-bridge and two boost half-bridges. This expansion can be realized in either a symmetric or asymmetric configuration. In the symmetric configuration, depicted in Fig. 13b, this extension to a six-switch buck-boost converter is applied to the three modules. In contrast, in the asymmetric configuration, the extension is applied only to selected modules, as illustrated in Fig. 13c, where it is applied solely to module a.

The Asymmetric Multiport Y-converter (AY-MPC) offers a more compact structure with fewer semiconductor devices and inductors compared to the Symmetric Multiport Y-converter (Y-MPC). When interlinking the three-phase ac grid with two dc systems operating at different power levels, the AY-MPC integrates the lower-power dc system into the grid using a minimal number of components, resulting in a simpler structure and a more compact overall size.

In the AY-MPC, module a comprises two inductors, L_1 and L_2, along with three half-bridges: one on the ac side, labeled Bu_a, and two on the dc sides, labeled Bo_{a1} and Bo_{a2}. In contrast, modules b and c each consist of a single inductor, L_1, and two half-bridges labeled Bu_b and Bo_{b1} for module b, and Bu_c and Bo_{c1} for module c.

The AY-MPC modules are interconnected at a central point, denoted as m, which serves as the neutral point for the Y-connection of the modules. Since each module operates as a dc-dc converter, it is essential to maintain a non-negative voltage on the ac side of each module ($v_{(a,b,c)m} \geq 0\,\text{V}$). To ensure this, an offset voltage between the grid neutral point n and m is required. A constant offset voltage, V_{off}, is applied, which must exceed the peak value of the ac grid phase voltage $\hat{V}_m$. The ac-side voltages v_{xm} can be mathematically

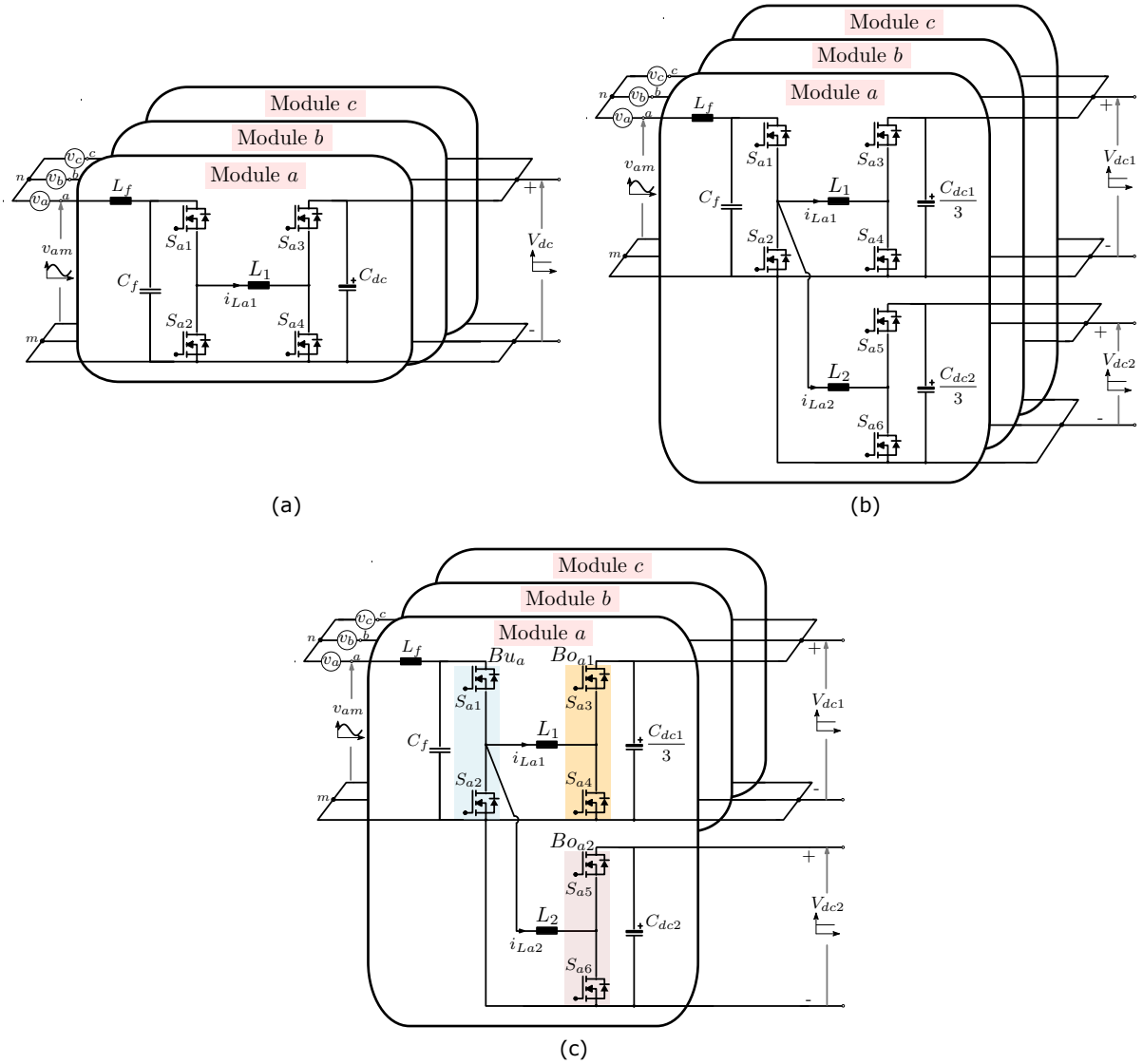


Figure 13: Different configurations of the modular Y-converter: (a) The two-port Y-converter, (b) The symmetric multiport Y-converter (Y-MPC), and (c) The asymmetric multiport Y-converter (AY-MPC).

expressed as:

$$v_{xm} = v_x + V_{off} = \hat{V}_m \sin(\omega t + \theta_x) + V_{\text{off}} \tag{11}$$

where v_x, with $x = (a, b, c)$, represents the ac grid phase voltages, ω denotes the ac grid frequency in rad/s, and θ_x signifies the respective phase angles of v_x.

In the subsequent analysis, two distinct operating modes of the AY-MPC are analyzed: Mode I, where the high-power port voltage V_{dc1} is lower than the low-power port voltage V_{dc2}, and Mode II, where V_{dc1} is higher than V_{dc2}. The key waveforms of the proposed AY-MPC in both modes are presented in Fig. 14.

4.1.1 Mode I ($V_{dc1} < V_{dc2}$)

In this mode, the Bu_x and Bo_{x1} half-bridges are controlled so that only one half-bridge in each module is modulated at any given time, while the other remains clamped based on the values of v_{xm} and V_{dc1}. Meanwhile, Bo_{a2} is modulated continuously.

In each module, when their ac-side voltage is greater than V_{dc1}, their corresponding Bu_x half-bridge keep switching, while their corresponding Bo_{x1} half-bridge is clamped with S_{x3} on and S_{x4} off. To determine the duty cycle of S_{x1}, denoted as d_{bu_x}, the following calculation can be applied:

$$d_{bu_x} = \frac{V_{dc1}}{v_{xm}} = \frac{V_{dc1}}{\hat{V}_m \sin(\omega t + \theta_x) + V_{off}} \tag{12}$$

For the Bo_{a2} half-bridge, it operates with a fixed duty cycle when v_{am} is greater than V_{dc1}, depending on the ratio between V_{dc1} and V_{dc2}. The duty cycle of S_{a5}, denoted as $d_{bo_{a2}}$, can be calculated as follows:

$$d_{bo_{a2}} = \frac{V_{dc1}}{V_{dc2}} \tag{13}$$

The ac grid currents, denoted as i_x, are assumed to be pure sinusoidal and in phase with its corresponding phase voltages v_x and then can be calculated as follows:

$$i_a = \hat{I}_m \sin(\omega t + \theta_x) = \frac{2(P_{dc1} + P_{dc2})}{3\hat{V}_m} \sin(\omega t + \theta_x) \tag{14}$$

where P_{dc1} and P_{dc2} represent the power delivered to dc port#1 and dc port#2, respectively, and $\hat{I}_m$ denotes the peak phase current.

By applying Kirchhoff's current law (KCL) at the ac input of each module, the average inductor currents, denoted as $i_{Lx_{av}}$, can be derived. For modules b and c, $i_{Lx_{av}}$ represents the average of their inductor currents, while for module a, it represents the average of the

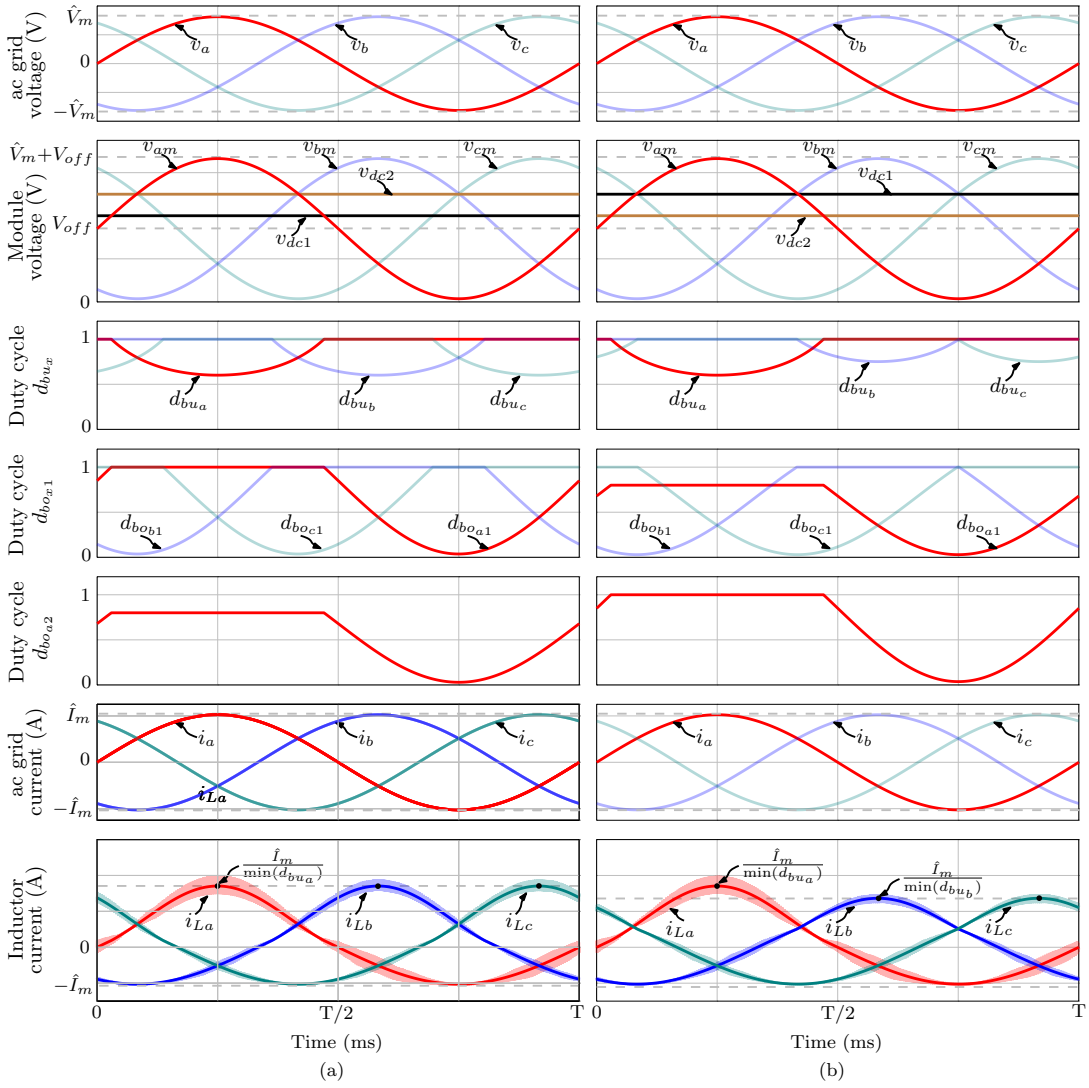


Figure 14: Key waveforms of the proposed AY-MPC in different operating modes: (a) Mode I: when V_{dc1} is lower than V_{dc2} and (b) Mode II: when V_{dc1} is greater than V_{dc2}.

sum of its two inductor currents. The relationship is given by:

$$i_{Lx_{av}} = \frac{i_x - i_{C_{f_x}}}{d_{bu_x}} \tag{15}$$

where $i_{C_{f_x}}$ represents the current through the input capacitor C_f. By neglecting $i_{C_{f_x}}$, the equation can be simplified as follows:

$$i_{Lx_{av}} = \frac{i_x}{d_{bu_x}} = \frac{\hat{I}_m \sin(\omega t + \theta_x)}{d_{bu_x}} \tag{16}$$

Similarly, for each module, when the ac-side voltage is lower than V_{dc1}, the corresponding Bo_{x1} half-bridge keeps switching, while the corresponding Bu_x half-bridge is clamped with S_{x1} on and S_{x2} off. To determine the duty cycle of S_{x3}, denoted as $d_{bo_{x1}}$, the following

calculation can be applied:

$$d_{bo_{x1}} = \frac{v_{xm}}{V_{dc1}} = \frac{\hat{V}_m \sin(\omega t + \theta_x) + V_{off}}{V_{dc1}} \tag{17}$$

For the Bo_{a2} half-bridge, $d_{bo_{a2}}$ can be calculated as follows:

$$d_{bo_{a2}} = \frac{v_{xm}}{V_{dc2}} = \frac{\hat{V}_m \sin(\omega t + \theta_x) + V_{off}}{V_{dc2}} \tag{18}$$

Using (16) and given that $d_{bu_x} = 1$, $i_{Lx_{av}}$ can be determined as:

$$i_{Lx_{av}} = i_x = \hat{I}_m \sin(\omega t + \theta_x) \tag{19}$$

The key waveforms of the proposed AY-MPC in Mode I are depicted in Fig. 14a. As evident from the analysis and waveforms, and given that V_{dc1}, which interconnects with the three modules, is lower than V_{dc2}, the converter exhibits symmetric duty cycles for the Bu_x and Bo_{x1} half-bridges. In fact, the Bu_x and Bo_{x1} half-bridges are modulated similarly to a conventional two-port Y-converter that interlinks the three-phase ac grid with V_{dc1}. Meanwhile, the Bo_{x2} half-bridge is continuously modulated throughout the entire cycle.

4.1.2 Mode II ($V_{dc1} > V_{dc2}$)

In this mode, where V_{dc2} is considered to be lower than V_{dc1}, the lower dc port voltage associated with module a is V_{dc2}, while modules b and c are only interconnected with V_{dc1}. As a result, the Bu_a half-bridge is controlled to step down v_{am} to V_{dc2} when v_{am} exceeds V_{dc2}. In contrast, modules b and c have their Bu_b and Bu_c half-bridges controlled to step down v_{bm} and v_{cm}, respectively, to V_{dc1}. This difference in the operation of the modules creates an asymmetry in the duty cycles of module a compared to modules b and c. As a result of this asymmetry, the following analysis will address each module's operation and its key relations individually.

For module a, when v_{am} exceeds V_{dc2}, the Bu_a half-bridge will be switching, while the Bo_{a2} half-bridge will remain clamped, with S_{a5} on and S_{a6} off. To determine d_{bu_a} in this mode, the following relationship can be used:

$$d_{bu_a} = \frac{V_{dc2}}{v_{am}} \tag{20}$$

For the Bo_{a1} half-bridge, $d_{bo_{a1}}$ can be calculated as follows:

$$d_{bo_{a1}} = \frac{V_{dc2}}{V_{dc1}} \tag{21}$$

Table 3: Summary of the basic equations of the proposed converter.

Parameter	Equation	Parameter	Equation
v_x	$\hat{V}_m \sin(\omega t + \theta_x)$	v_{xm}	$v_x + V_{\text{off}}$
d_{Bu_a}	$\frac{\min(v_{am}, V_{dc1}, V_{dc2})}{v_{am}}$	$d_{Bo_{a1}}$	$\frac{\min(v_{am}, V_{dc1}, V_{dc2})}{V_{dc1}}$
d_{Bu_b}	$\frac{\min(v_{bm}, V_{dc1})}{v_{bm}}$	$d_{Bo_{b1}}$	$\frac{\min(v_{bm}, V_{dc1})}{V_{dc1}}$
d_{Bu_c}	$\frac{\min(v_{cm}, V_{dc1})}{v_{cm}}$	$d_{Bo_{c1}}$	$\frac{\min(v_{cm}, V_{dc1})}{V_{dc1}}$
$d_{Bo_{a2}}$	$\frac{\min(v_{am}, V_{dc1}, V_{dc2})}{V_{dc2}}$	$i_{Lx_{av}}$	$\frac{\hat{I}_m \sin(\omega t + \theta_x)}{d_{Bu_x}}$

When v_{am} is lower than V_{dc2}, the Bo_{a1} and Bo_{a2} half-bridges will be switching, while the Bu_a half-bridge will be clamped with S_{a1} on and S_{a2} off. To determine $d_{bo_{a1}}$ and $d_{bo_{a2}}$ in this mode, the following calculations can be applied:

$$d_{bo_{a1}} = \frac{v_{am}}{V_{dc1}}, \quad d_{bo_{a2}} = \frac{v_{am}}{V_{dc2}} \tag{22}$$

For modules b and c, operation remains consistent in both Mode I and Mode II, as the functioning of their half-bridges depends only on V_{dc1}, v_{bm}, and v_{cm}. Consequently, the modulation strategy and key relations given in (12) and (17) for Mode I are also applicable to Mode II.

The key waveforms of the proposed AY-MPC in Mode II are presented in Fig. 14b. As highlighted in the previous analysis, the converter exhibits asymmetric duty cycles for the half-bridges in different modules, resulting in asymmetry in the i_{Lx} currents. In addition to the key waveforms, the fundamental equations governing the proposed converter, applicable to both Mode I and Mode II, are summarized in Table 3.

4.2 Minimization of the Low-frequency Voltage Ripples at the DC ports

The AY-MPC offers a reduced structure compared to the Y-MPC, which potentially leads to a more compact and lower-cost power converter, especially when interfacing two dc ports with high and low power levels. However, two challenges arise with the AY-MPC: maintaining balanced ac grid currents given the asymmetric structure, and minimizing low-frequency voltage ripples at the dc ports. These ripples appear on V_{dc2} due to the single-phase power flow from the ac grid, similar to any typical single-phase rectifier, and on V_{dc1} due to the unbalanced power flow from the ac grid to V_{dc1} across the three modules.

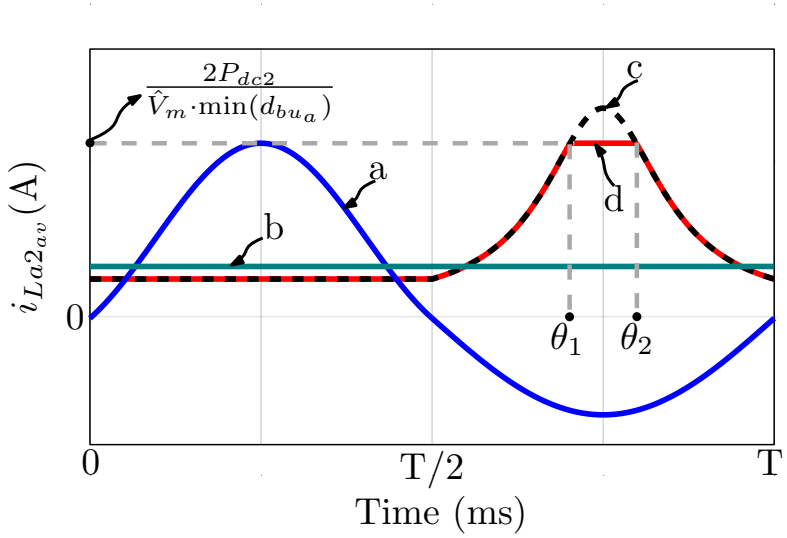


Figure 15: Different waveforms of $i_{La2_{av}}$ to be analyzed for reducing the low-frequency voltage ripples at the dc ports: (a) original waveform; (b) dc waveform; (c) ideal waveform eliminating the low-frequency voltage ripples; and (d) clamped waveform. The waveforms are not to scale.

To address both challenges, $i_{La1_{av}}$ and $i_{La2_{av}}$ are controlled to ensure balanced ac grid currents and minimized low-frequency voltage ripples at the dc ports. To achieve balanced ac grid currents, the sum of $i_{La1_{av}}$ and $i_{La2_{av}}$ is controlled to be equal to $i_{La_{av}}$, as indicated in (16). Additionally, a new degree of freedom is introduced: the ability to shape both $i_{La1_{av}}$ and $i_{La2_{av}}$ while ensuring their sum equals $i_{La_{av}}$. This degree of freedom is utilized to minimize the low-frequency voltage ripples at the dc ports.

Theoretically, despite the asymmetric structure, the low-frequency voltage ripples at the dc ports can be effectively eliminated. Assuming a ripple-free dc current at dc port #2, denoted as I_{dc2}, the resulting $i_{La2_{av}}$ is calculated as follows:

$$i_{La2_{av}} = \frac{I_{dc2}}{d_{bo_{a2}}} \tag{23}$$

As $d_{bo_{a2}}$ tends to zero when v_a is at its minimum value, shaping $i_{La2_{av}}$ to fully eliminate the low-frequency voltage ripples at the dc ports leads to excessive current stresses on the semiconductor devices and inductors of module a. Although these excessive current stresses can be reduced by increasing V_{off}, the overall performance of the converter will be degraded due to the increased voltage and current stresses across all modules. Therefore, in the following analysis, shaping $i_{La2_{av}}$ to fully eliminate the low-frequency voltage ripples at the dc ports will not be considered. Instead, three different waveforms of $i_{La2_{av}}$ are analyzed with the aim of minimizing the voltage ripples without significantly increasing the current stresses on the AY-MPC components. These $i_{La2_{av}}$ waveforms are presented in Fig. 15.

The first waveform of $i_{La2_{av}}$ resembles the shape of $i_{La_{av}}$ (also the inductor current of the two-port Y-converter) and will therefore be referred to in the following discussion as the original waveform. The $i_{La2_{av}}$ in this case can be determined as follows:

$$i_{La2_{av}} = \frac{2P_{dc2}}{\hat{V}_m \cdot d_{bu_a}} \sin(\omega t) \tag{24}$$

The second waveform of $i_{La2_{av}}$ is a dc waveform, where the magnitude of this dc waveform is controlled to deliver the required P_{dc2}. Lastly, the third waveform of $i_{La2_{av}}$ modifies the waveform presented in (23), which ideally eliminates the voltage ripples, into a clamped waveform where the peak current is limited to a specific value. This waveform will be referred to in the following discussion as the clamped waveform, and the peak value is selected to be equal to the peak of the original waveform presented in (24). The $i_{La2_{av}}$ in this case can be determined as follows:

$$i_{La2_{av}} = \min\left(\frac{2P_{dc2}}{\hat{V}_m \cdot \min(d_{bu_a})}, \frac{I_{dc2}}{d_{bo_{a2}}}\right) \tag{25}$$

For each $i_{La2_{av}}$ waveform presented in Fig. 15, the corresponding $i_{La1_{av}}$ waveform must also be adjusted to maintain balanced ac grid currents. The three $i_{La2_{av}}$ waveforms, along with their respective $i_{La1_{av}}$ waveforms, are shown in Fig. 16. In these waveforms, V_{dc1} and V_{dc2} are set to $400\,\text{V}$ and $500\,\text{V}$, respectively, while P_{dc1} and P_{dc2} are set to $3\,\text{kW}$ and $1\,\text{kW}$, respectively.

To demonstrate the performance of the three $i_{La2_{av}}$ waveforms, the required capacitance at dc port #2, denoted as C_{dc2}, to attain a $10\,\text{V}$ peak-to-peak voltage ripple at V_{dc2} is defined using numerical simulations. Fig. 17 presents the required C_{dc2} for the three $i_{La2_{av}}$ waveforms, with V_{dc2} ranging from $450\,\text{V}$ to $800\,\text{V}$, while V_{dc1} is fixed at $400\,\text{V}$, and P_{dc1} and P_{dc2} are set to $3\,\text{kW}$ and $1\,\text{kW}$, respectively. The results highlight the reduction in C_{dc2} when using the dc or clamped waveform compared to the original waveform. For instance, at V_{dc2} equal to $450\,\text{V}$, the required C_{dc2} values are $3.18\,\text{mF}$, $1.14\,\text{mF}$, and $0.56\,\text{mF}$ for the original, dc, and clamped waveforms, respectively. Beside the dependence of the required C_{dc2} on the V_{dc2}, the required C_{dc2} varies linearly with P_{dc2}.

4.3 Experimental Results

The AY-MPC prototype can be considered a reduced version of the Y-MPC prototype shown in Fig. 9. The AY-MPC prototype is constructed by combining four Imperix PEB8024 half-bridge power modules with C2M0080120D SiC MOSFETs for the dc-side half-bridges (instead of six modules used in the Y-MPC prototype), while the ac-side half-bridges are implemented with UF4SC120023K4S SiC MOSFETs, which feature a lower R_{ds} compared to the dc-side devices due to higher current stresses. Control of the prototype is achieved using only

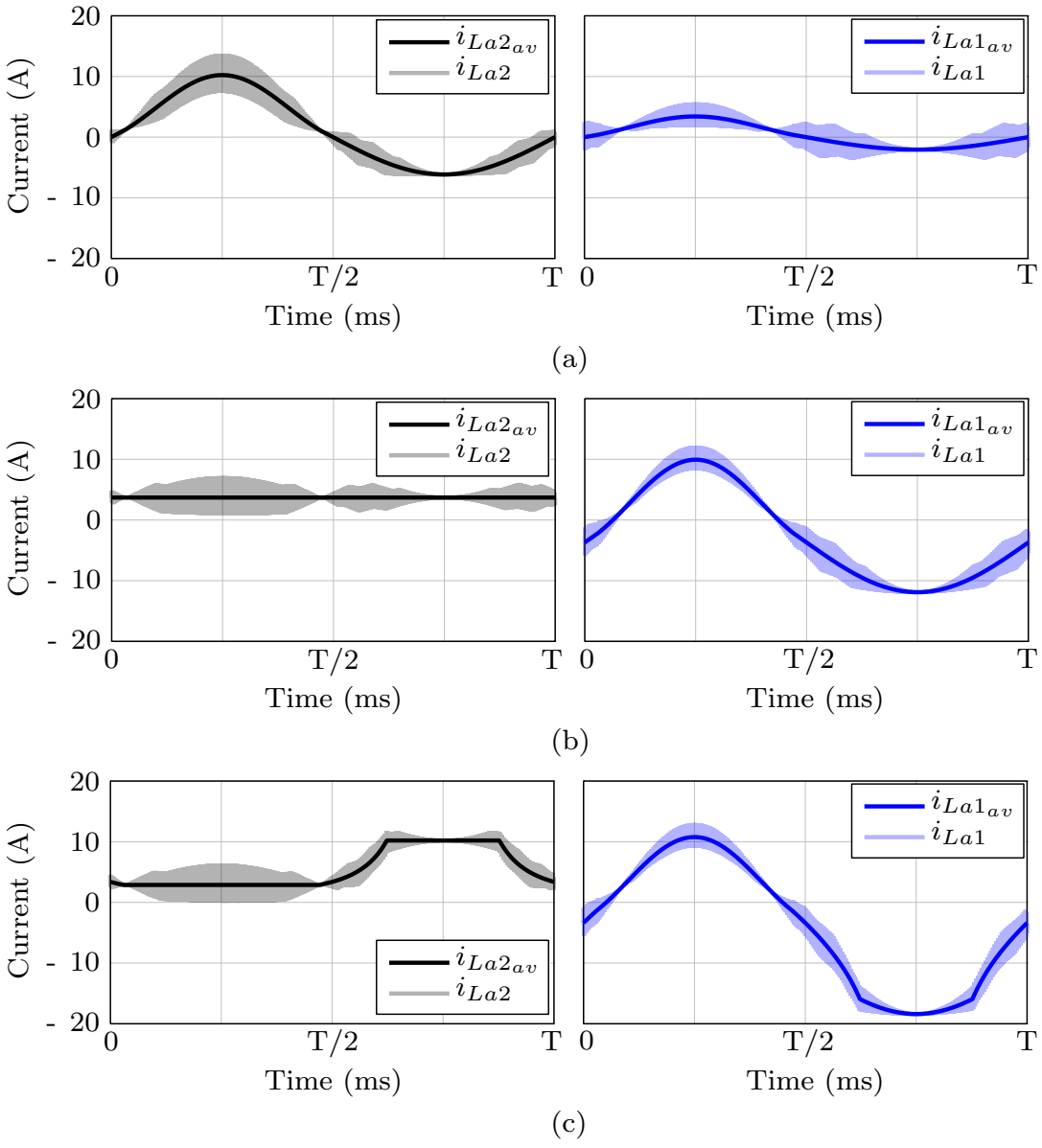


Figure 16: Different waveforms of i_{La2} and their corresponding i_{La1} to to maintain balanced ac grid currents: (a) i_{La2} original waveform; (b) i_{La2} dc waveform; and (c) i_{La2} clamped waveform.

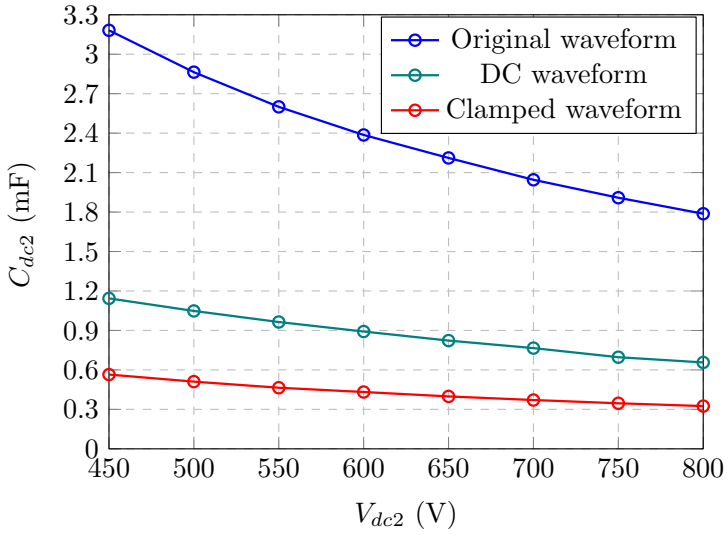


Figure 17: Required C_{dc2} for the three $i_{La2_{av}}$ waveforms with V_{dc1} is fixed at $400\,\text{V}$, P_{dc1} and P_{dc2} are set to $3\,\text{kW}$ and $1\,\text{kW}$, respectively.

one B-box controller, compared to the two B-box controllers used in the Y-MPC prototype. Bidirectional ac and dc power supplies are employed to emulate the ac grid and dc MGs. L_1 and L_2 are implemented using $330\,\mu\text{H}$ inductors, and a single-stage input filter is utilized with $L_f = 1.2\,\text{mH}$ and $C_f = 10\,\mu\text{F}$.

The following experimental results are categorized into three sections: steady-state results, transient results, and efficiency evaluation results. In these sections, the performance is examined in both Mode I and Mode II. Additionally, the converter's performance with the three $i_{La2_{av}}$ waveforms is demonstrated.

4.4 Steady-State Experimental Results

This section presents experimental waveforms to demonstrate the converter's performance in steady-state under various operating modes and $i_{La2_{av}}$ waveforms. Additionally, the results showcase the converter's behavior at different values of P_{dc1} and P_{dc2}, providing insights into its steady-state performance under varying power conditions.

4.4.1 Mode I ($V_{dc1} < V_{dc2}$)

In Mode I, when V_{dc1} is lower than V_{dc2}, the operating conditions are set as follows: V_{dc1} is maintained at $400\,\text{V}$ and V_{dc2} at $500\,\text{V}$, with the ac grid voltage set to its rated value. This conditions serve as baselines for the experimental results presented in Mode I.

Experimental waveforms of the AY-MPC prototype, in Mode I and with the original $i_{La2_{av}}$ waveform, are presented in Fig. 18 to showcase its performance under different operating conditions. The first operating point is displayed in Fig. 18a, where P_{dc1} equals $3\,\text{kW}$ and P_{dc2} equals $0.5\,\text{kW}$. As evident from the waveforms, the experimental results match the analysis

and simulations, showing pure sinusoidal ac grid currents that are well-synchronized with the ac voltages, resulting in a measured power factor above 0.99. Additionally, despite the asymmetric structure of the proposed converter, the ac currents remain balanced.

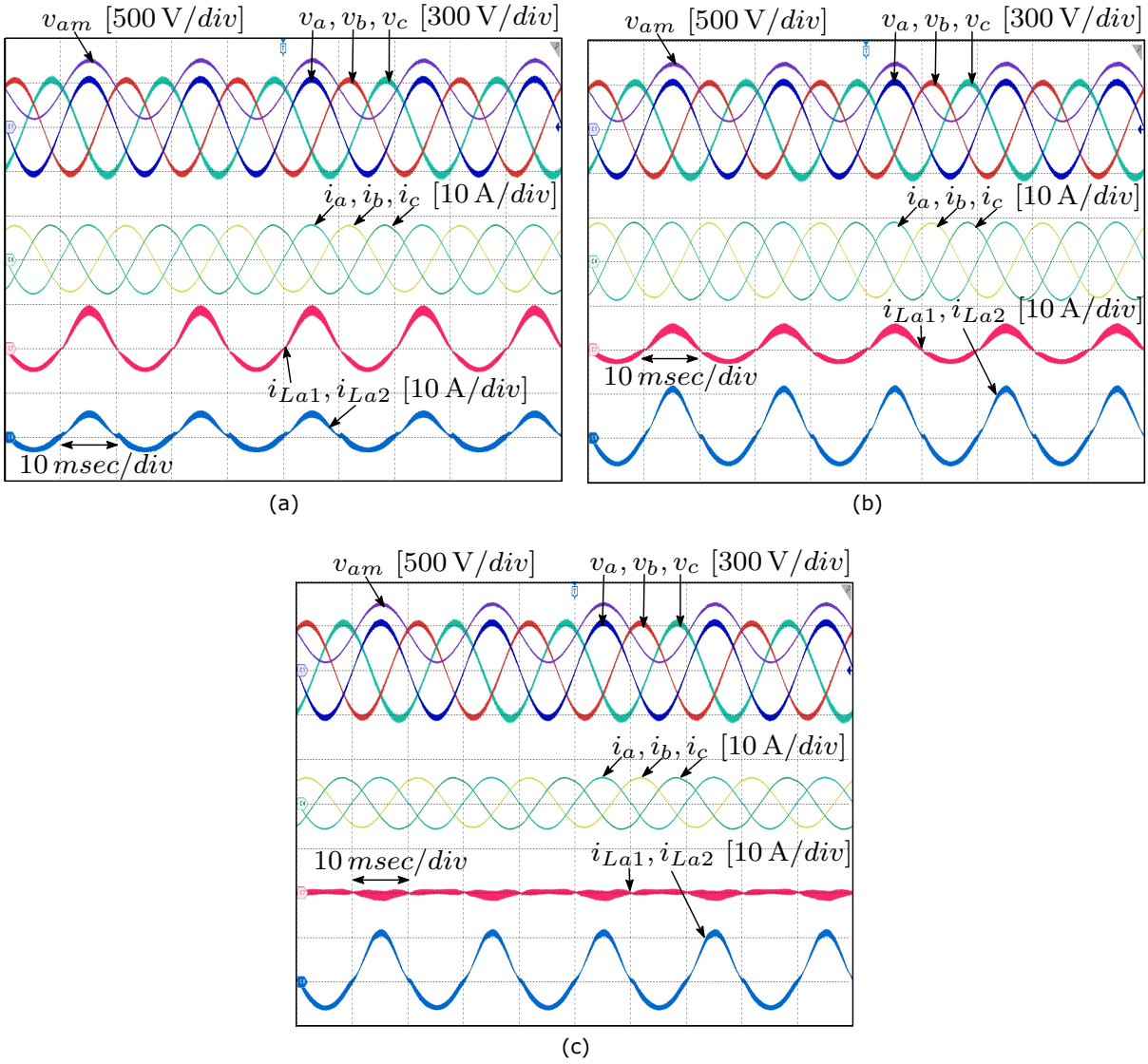


Figure 18: Experimental waveforms of the proposed converter in Mode I, using the original $i_{La2_{av}}$ waveform at different power levels, with V_{dc1} and V_{dc2} set to $400\,\text{V}$ and $500\,\text{V}$, respectively: (a) P_{dc1} equals $3\,\text{kW}$ and P_{dc2} equals $0.5\,\text{kW}$; (b) P_{dc1} equals $3\,\text{kW}$ and P_{dc2} equals $1\,\text{kW}$; and (c) P_{dc1} equals $1.6\,\text{kW}$ and P_{dc2} equals $1\,\text{kW}$.

The second operating point is displayed in Fig. 18b, where P_{dc1} equals $3\,\text{kW}$ and P_{dc2} equals $1\,\text{kW}$. Compared to the first operating point, P_{dc2} is increased from $0.5\,\text{kW}$ to $1\,\text{kW}$. Consequently, i_{La2} increases to deliver the required P_{dc2}, while i_{La1} decreases to maintain balanced ac grid currents. Similarly, in the third operating point, presented in Fig. 18c, where P_{dc1} equals $1.6\,\text{kW}$ and P_{dc2} equals $1\,\text{kW}$, as P_{dc1} decreases compared to the previous operating conditions, i_{La1} further decreases to maintain balanced ac grid currents. As

demonstrated in the three operating conditions, pure sinusoidal ac grid currents that are well-synchronized with the ac voltages are attained at different power levels.

The experimental waveforms of the proposed AY-MPC, operating in Mode I with the dc $i_{La2_{av}}$ waveform, are presented in Fig. 19. The first operating point is shown in Fig. 19a, where P_{dc1} equals $1.6\,$kW and P_{dc2} equals $1\,$kW. The second operating point, displayed in Fig. 19b, features P_{dc1} at $3\,$kW and P_{dc2} at $1\,$kW. The third operating point, presented in Fig. 19c, shows P_{dc1} at $1.6\,$kW and P_{dc2} at $1\,$kW. The experimental waveforms demonstrate the effective shaping of both i_{La1} and i_{La2}, which minimizes low-frequency voltage ripples at the dc ports while maintaining pure sinusoidal and balanced ac grid currents. As evident from the results reported in Fig. 18 and Fig. 19, the quality of the ac grid currents is not affected by the selected $i_{La2_{av}}$ waveform.

Fig. 20 displays the experimental waveforms of the proposed AY-MPC, operating in Mode I with the clamped $i_{La2_{av}}$ waveform. The first operating point is shown in Fig. 20a, where P_{dc1} equals $1.6\,$kW and P_{dc2} equals $1\,$kW. The second operating point, displayed in Fig. 20b, features P_{dc1} at $3\,$kW and P_{dc2} at $1\,$kW. The third operating point, presented in Fig. 20c, shows P_{dc1} at $1.6\,$kW and P_{dc2} at $1\,$kW. The experimental waveforms demonstrate effective shaping of both i_{La1} and i_{La2}, as well as the successful limiting of i_{La2} according to (25), preventing excessive currents in module a devices. Once again, as evident from the results reported in Fig. 18, Fig. 19, and Fig. 20, the quality of the ac grid currents remains unaffected by the selected $i_{La2_{av}}$ waveform.

4.4.2 Mode II ($V_{dc1} > V_{dc2}$)

In Mode II, when V_{dc1} is higher than V_{dc2}, the operating conditions are set as follows: V_{dc1} is maintained at $500\,$V and V_{dc2} at $400\,$V, with the ac grid voltage set to its rated value. This conditions serve as baselines for the experimental results presented in Mode II.

Experimental waveforms of the AY-MPC prototype in Mode II, using the original $i_{La2_{av}}$ waveform, are shown in Fig. 21. In both presented operating points, V_{dc1} is set to $500\,$V and V_{dc2} to $400\,$V. The first operating point, presented in Fig. 21a, corresponds to P_{dc1} of $3\,$kW and P_{dc2} of $0.5\,$kW. The second operating point, shown in Fig. 21b, corresponds to P_{dc1} of $3\,$kW and P_{dc2} of $1\,$kW.

The waveforms confirm that the proposed converter operates efficiently in both Mode I and Mode II, with experimental results aligning with analytical and simulation findings. The balanced, pure sinusoidal ac grid currents are synchronized with the ac voltages, delivering a measured power factor exceeding 0.99.

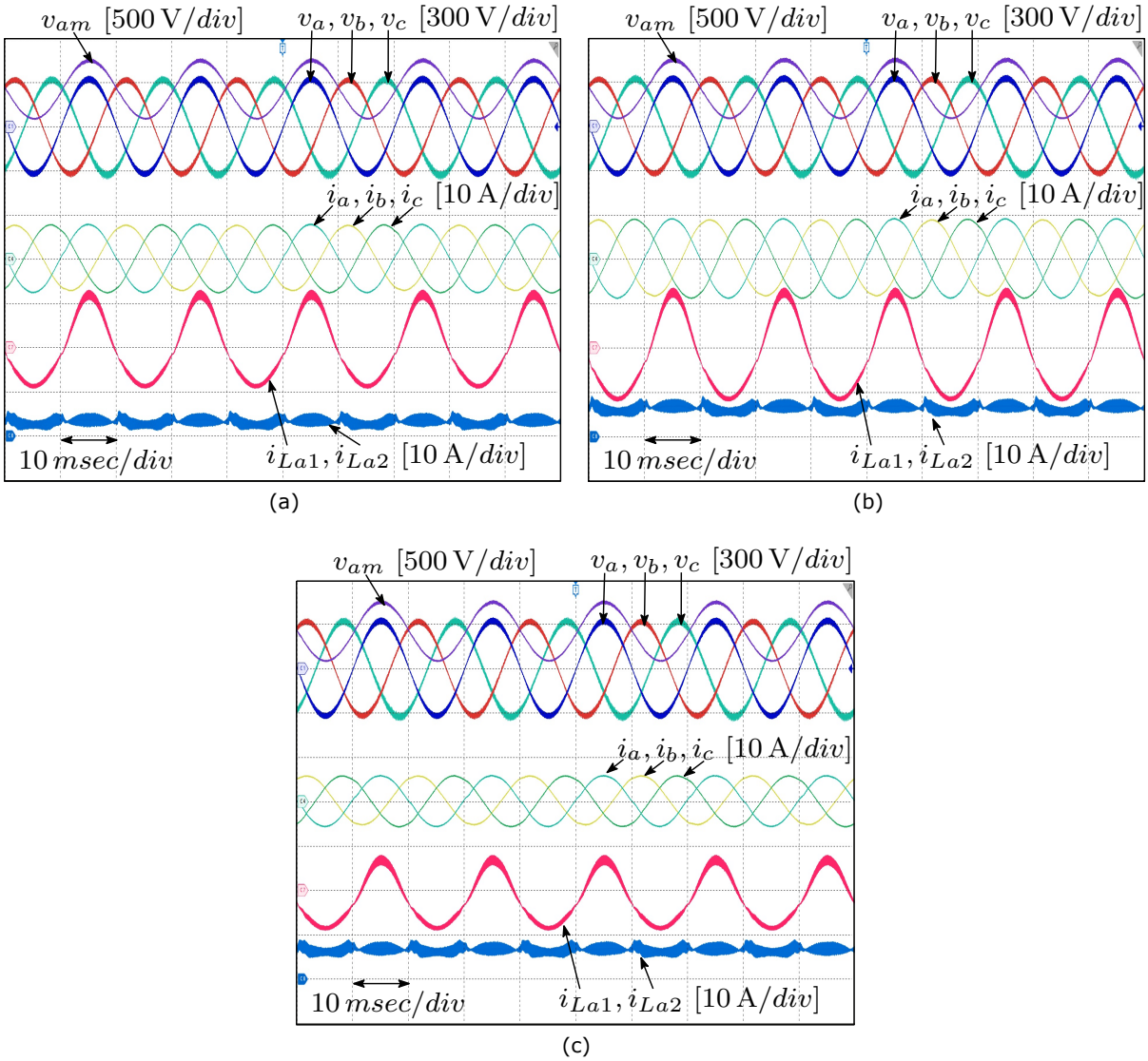


Figure 19: Experimental waveforms of the proposed converter in Mode I, using the dc $i_{La2_{av}}$ waveform at different power levels, with V_{dc1} and V_{dc2} set to 400 V and 500 V, respectively: (a) P_{dc1} equals 3 kW and P_{dc2} equals 0.5 kW; (b) P_{dc1} equals 3 kW and P_{dc2} equals 1 kW; and (c) P_{dc1} equals 1.6 kW and P_{dc2} equals 1 kW.

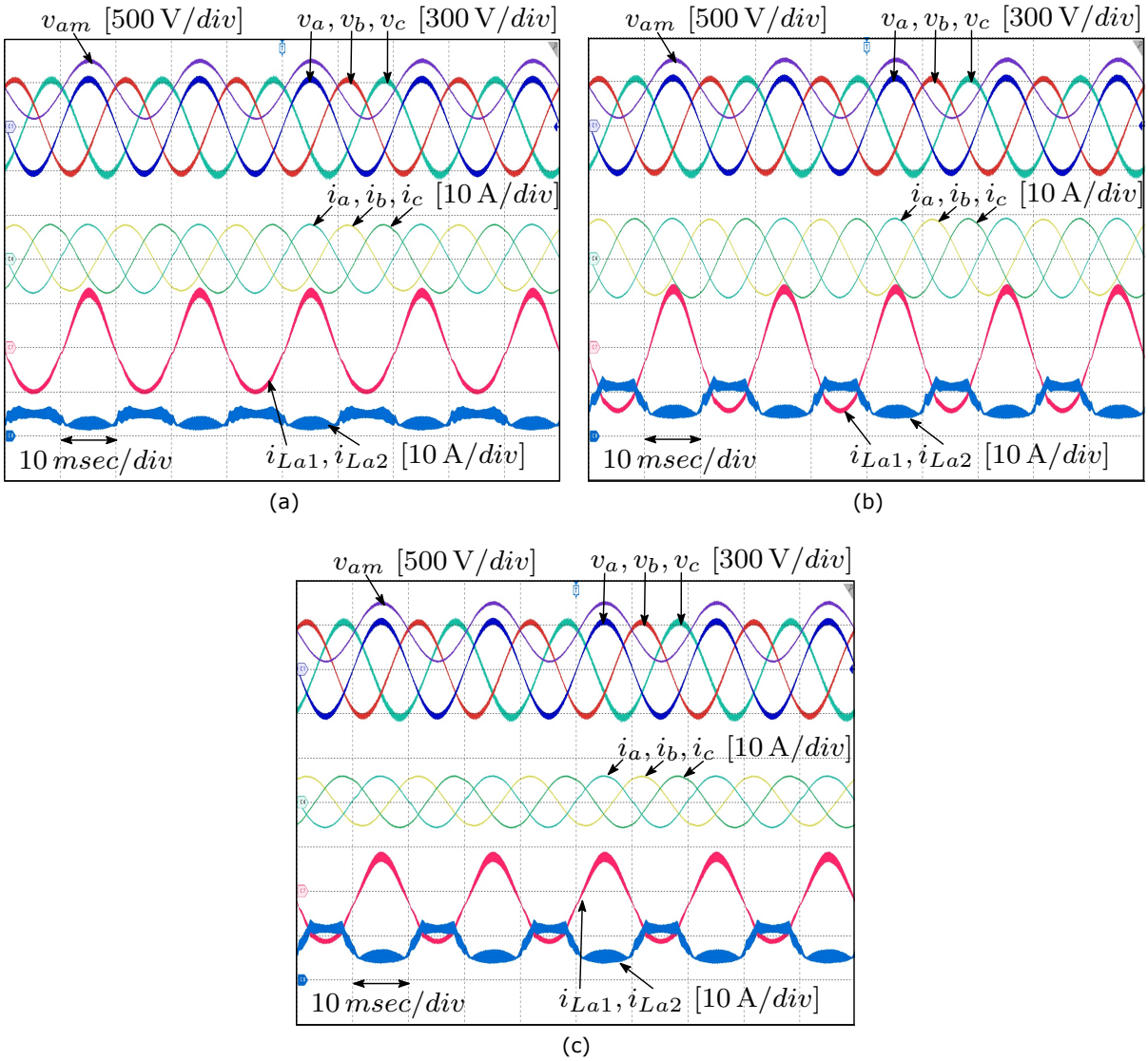


Figure 20: Experimental waveforms of the proposed converter in Mode I, using the clamped $i_{La2_{av}}$ waveform at different power levels, with V_{dc1} and V_{dc2} set to $400\,\text{V}$ and $500\,\text{V}$, respectively: (a) P_{dc1} equals $3\,\text{kW}$ and P_{dc2} equals $0.5\,\text{kW}$; (b) P_{dc1} equals $3\,\text{kW}$ and P_{dc2} equals $1\,\text{kW}$; and (c) P_{dc1} equals $1.6\,\text{kW}$ and P_{dc2} equals $1\,\text{kW}$.

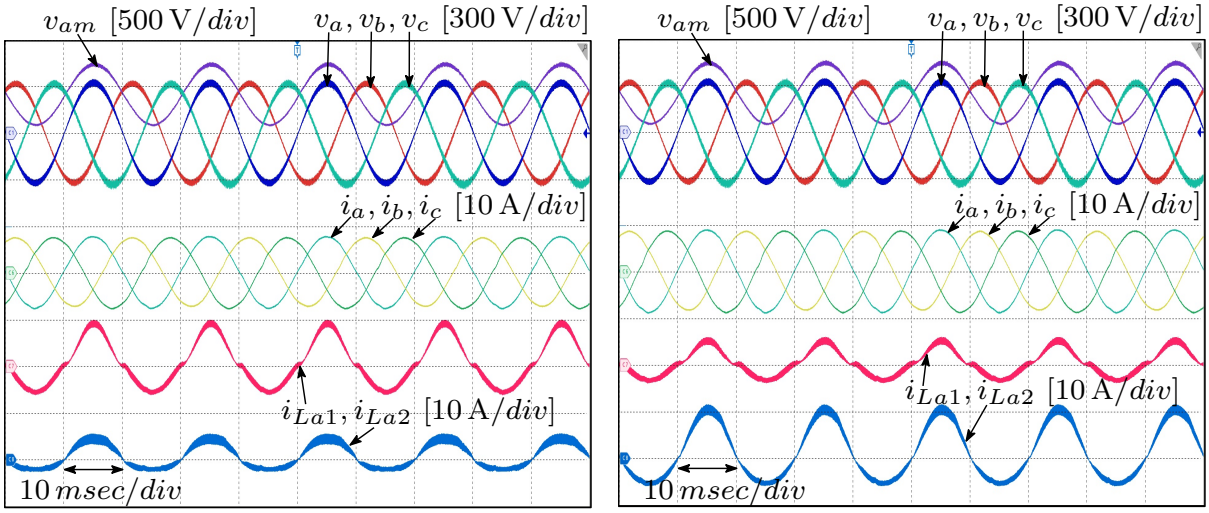


Figure 21: Experimental waveforms of the proposed converter in Mode II, using the original $i_{La2_{av}}$ waveform at different power levels, with V_{dc1} and V_{dc2} set to $400\,\text{V}$ and $500\,\text{V}$, respectively: (a) P_{dc1} equals $3\,\text{kW}$ and P_{dc2} equals $0.5\,\text{kW}$; and (b) P_{dc1} equals $3\,\text{kW}$ and P_{dc2} equals $1\,\text{kW}$.

4.4.3 Transient Experimental Results

This section evaluates the transient behavior of the proposed AY-MPC converter under variations in P_{dc1} and P_{dc2}. The objective is to demonstrate the robustness of the adopted control technique and to provide deeper insights into the converter's performance across different operating modes. By analyzing the converter's response to changes in power levels, the section highlights its stability and ability to maintain high-quality performance during dynamic operating conditions. The results presented will focus on both Mode I and Mode II, showcasing the converter's resilience and fast response to power transients.

4.4.3.1 Mode I ($V_{dc1} < V_{dc2}$) The transient behavior of the AY-MPC is examined in Mode I with the original $i_{La2_{av}}$ waveform, where V_{dc1} equals $400\,\text{V}$ and V_{dc2} equals $500\,\text{V}$. The transient response is first assessed by varying P_{dc1} while keeping P_{dc2} constant. In Fig. 22a, the converter's transient performance is shown as P_{dc1} is increased from $1\,\text{kW}$ to $3\,\text{kW}$, with P_{dc2} held constant at $0.5\,\text{kW}$. While in Fig. 22b, the transient performance is presented for the reverse scenario, where P_{dc1} is decreased from $3\,\text{kW}$ to $1\,\text{kW}$, again with P_{dc2} kept constant at $0.5\,\text{kW}$.

The waveforms demonstrate the smooth transition and the converter's ability to maintain pure sinusoidal ac grid currents, despite both the increase and decrease in P_{dc1}. Additionally, P_{dc2} remains unaffected by the transient changes in P_{dc1}, as evident from the unchanged i_{La2} waveform. This highlights the effective power decoupling between P_{dc1} and P_{dc2}, ensuring stable operation across different power conditions.

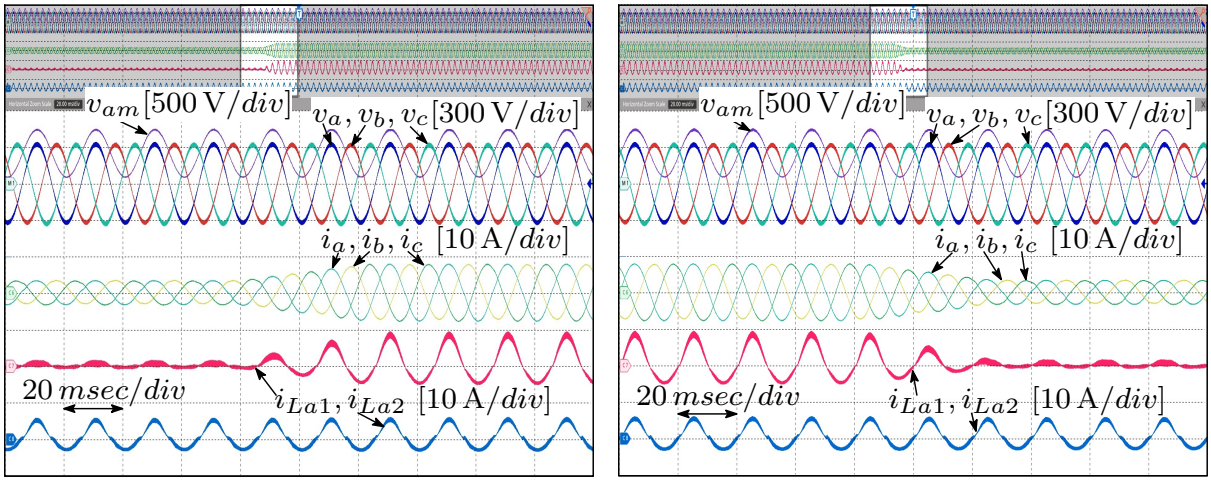


Figure 22: Experimental waveforms illustrating the transient behavior of the proposed converter in Mode I with the original $i_{La2_{av}}$ waveform at V_{dc1} equals $400\,\text{V}$, V_{dc2} equals $500\,\text{V}$, and P_{dc1} equals $0.5\,\text{kW}$: (a) P_{dc1} is increased from $1\,\text{kW}$ to $3\,\text{kW}$; and (b) P_{dc1} is decreased from $3\,\text{kW}$ to $1\,\text{kW}$.

To demonstrate the transient response when P_{dc2} is varied while keeping P_{dc1} constant, Fig. 23a presents the converter's waveforms during the transient when P_{dc2} is increased from $0.1\,\text{kW}$ to $1\,\text{kW}$, with P_{dc1} held constant at $3\,\text{kW}$. Additionally, Fig. 23b presents the transient performance for the reverse scenario, where P_{dc2} is decreased from $1\,\text{kW}$ to $0.1\,\text{kW}$, again with P_{dc1} kept constant at $3\,\text{kW}$.

The waveforms again showcase the seamless, stable transition and the converter's ability to maintain pure sinusoidal ac grid currents, despite both the increase and decrease in P_{dc2}. Additionally, the change in i_{La1} to maintain balanced ac grid currents is evident. It is worth highlighting that P_{dc1} remains constant and unaffected by the transient changes in P_{dc2}. Although i_{La1} varies with the change in i_{La2}, modules b and c are controlled to compensate for this variation, ensuring smooth operation.

The transient behavior of the AY-MPC is also examined in Mode I with the dc $i_{La2_{av}}$ waveform. The same conditions as in the original $i_{La2_{av}}$ waveform are applied, with V_{dc1} set to $400\,\text{V}$ and V_{dc2} set to $500\,\text{V}$. In Fig. 24a, the converter's transient performance is demonstrated as P_{dc1} increases from $1\,\text{kW}$ to $3\,\text{kW}$, while P_{dc2} is maintained at $0.5\,\text{kW}$. In Fig. 24b, the reverse scenario is presented, where P_{dc1} decreases from $3\,\text{kW}$ to $1\,\text{kW}$, with P_{dc2} still held constant at $0.5\,\text{kW}$.

Similarly, the transient performance is assessed when P_{dc2} is varied while keeping P_{dc1} constant. Fig. 25a presents the converter's waveforms during the transient when P_{dc2} is increased from $0.1\,\text{kW}$ to $1\,\text{kW}$, with P_{dc1} held constant at $3\,\text{kW}$. Additionally, Fig. 25b shows the transient performance for the reverse scenario, where P_{dc2} decreases from $1\,\text{kW}$ to $0.1\,\text{kW}$, with P_{dc1} still kept constant at $3\,\text{kW}$.

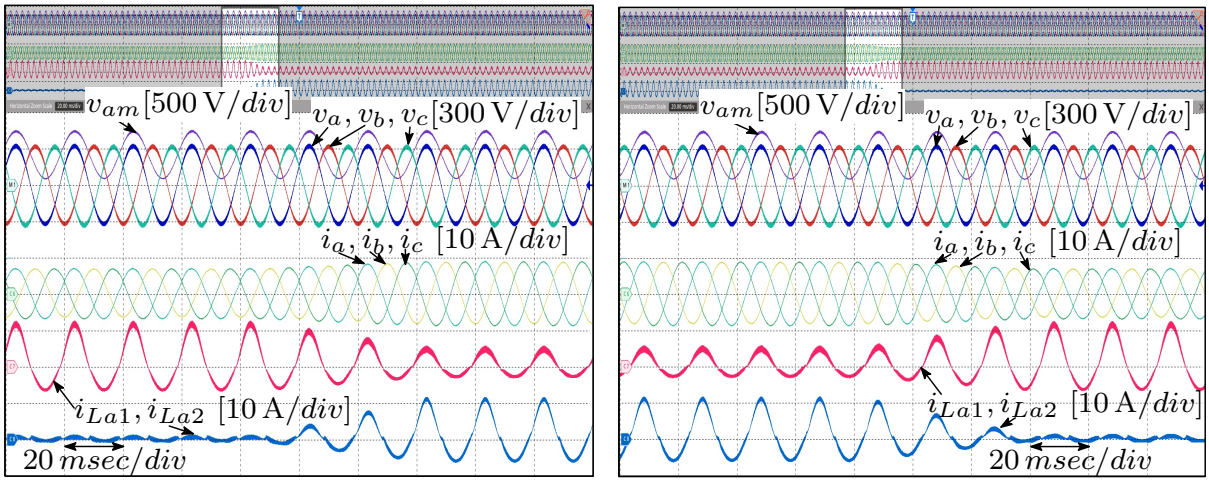


Figure 23: Experimental waveforms illustrating the transient behavior of the proposed converter in Mode I with the original $i_{La2_{av}}$ waveform at V_{dc1} equals 400 V, V_{dc2} equals 500 V, and P_{dc1} equals 3 kW: (a) P_{dc2} is increased from 0.1 kW to 1 kW; and (b) P_{dc2} is decreased from 1 kW to 0.1 kW.

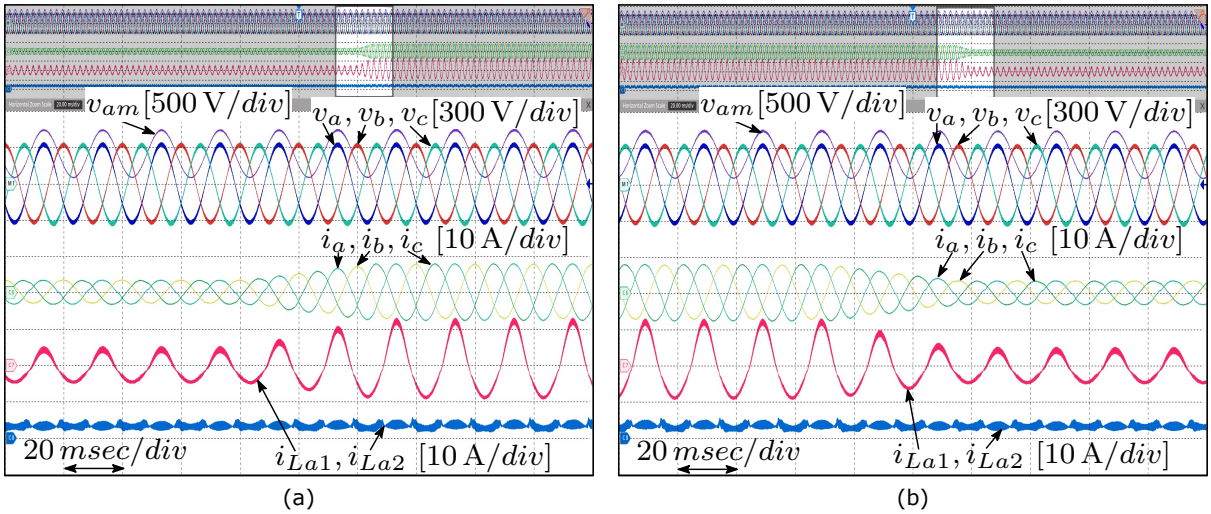


Figure 24: Experimental waveforms illustrating the transient behavior of the proposed converter in Mode I with the dc $i_{La2_{av}}$ waveform at V_{dc1} equals 400 V, V_{dc2} equals 500 V, and P_{dc1} equals 0.5 kW: (a) P_{dc1} is increased from 1 kW to 3 kW; and (b) P_{dc1} is decreased from 3 kW to 1 kW.

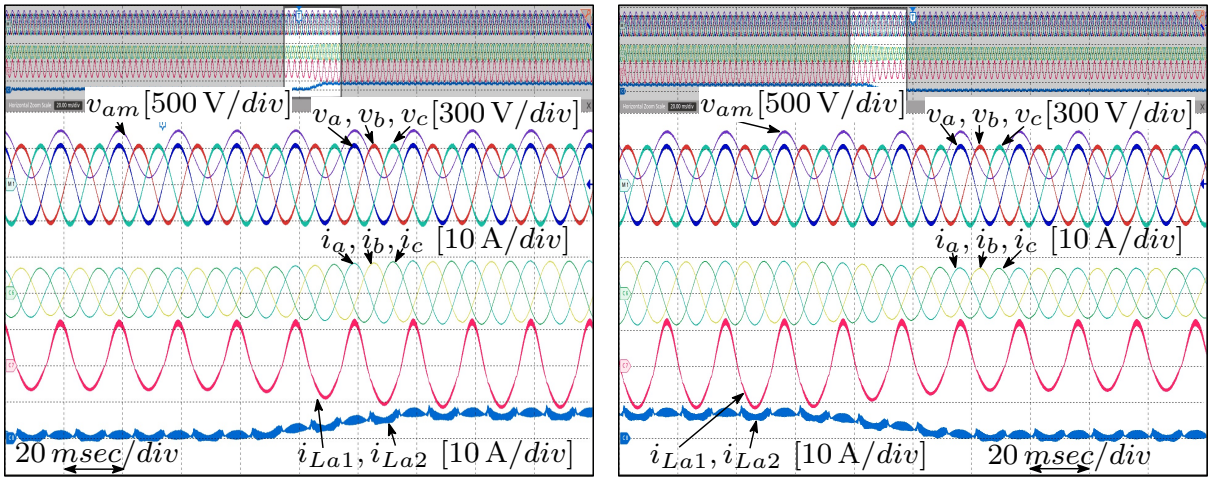


Figure 25: Experimental waveforms illustrating the transient behavior of the proposed converter in Mode I with the dc $i_{La2_{av}}$ waveform at V_{dc1} equals $400\,\mathrm{V}$, V_{dc2} equals $500\,\mathrm{V}$, and P_{dc1} equals $3\,\mathrm{kW}$: (a) P_{dc2} is increased from $0.1\,\mathrm{kW}$ to $1\,\mathrm{kW}$; and (b) P_{dc2} is decreased from $1\,\mathrm{kW}$ to $0.1\,\mathrm{kW}$.

Lastly, the transient behavior of the AY-MPC is examined in Mode I with the clamped $i_{La2_{av}}$ waveform. In Fig. 26a, the converter's transient performance is demonstrated as P_{dc1} increases from $1\,\mathrm{kW}$ to $3\,\mathrm{kW}$, while P_{dc2} is maintained at $0.5\,\mathrm{kW}$. In Fig. 26b, the reverse scenario is presented, where P_{dc1} decreases from $3\,\mathrm{kW}$ to $1\,\mathrm{kW}$, with P_{dc2} still held constant at $0.5\,\mathrm{kW}$.

Fig. 27a presents the converter's waveforms during the transient when P_{dc2} is increased from $0.1\,\mathrm{kW}$ to $1\,\mathrm{kW}$, with P_{dc1} held constant at $3\,\mathrm{kW}$. Additionally, Fig. 27b shows the transient performance for the reverse scenario, where P_{dc2} is decreased from $1\,\mathrm{kW}$ to $0.1\,\mathrm{kW}$, again with P_{dc1} kept constant at $3\,\mathrm{kW}$.

4.4.4 Mode II ($V_{dc1} > V_{dc2}$)

The transient behavior of the AY-MPC is analyzed in Mode II with the original $i_{La2_{av}}$ waveform, where V_{dc1} equals $500\,\mathrm{V}$ and V_{dc2} equals $400\,\mathrm{V}$. The transient response is first evaluated by varying P_{dc1} while maintaining P_{dc2} constant.

In Fig. 28a, the converter's transient performance is illustrated as P_{dc1} increases from $1\,\mathrm{kW}$ to $3\,\mathrm{kW}$, with P_{dc2} fixed at $0.5\,\mathrm{kW}$. Conversely, Fig. 28b shows the transient performance when P_{dc1} decreases from $3\,\mathrm{kW}$ to $1\,\mathrm{kW}$, again with P_{dc2} held constant at $0.5\,\mathrm{kW}$.

To demonstrate the transient response when P_{dc2} is varied while P_{dc1} remains constant, Fig. 29a displays the converter's waveforms during the transition as P_{dc2} increases from $0.1\,\mathrm{kW}$ to $1\,\mathrm{kW}$, with P_{dc1} held steady at $3\,\mathrm{kW}$. Additionally, Fig. 29b illustrates the transient performance for the reverse scenario, where P_{dc2} decreases from $1\,\mathrm{kW}$ to $0.1\,\mathrm{kW}$, while P_{dc1} remains constant at $3\,\mathrm{kW}$.

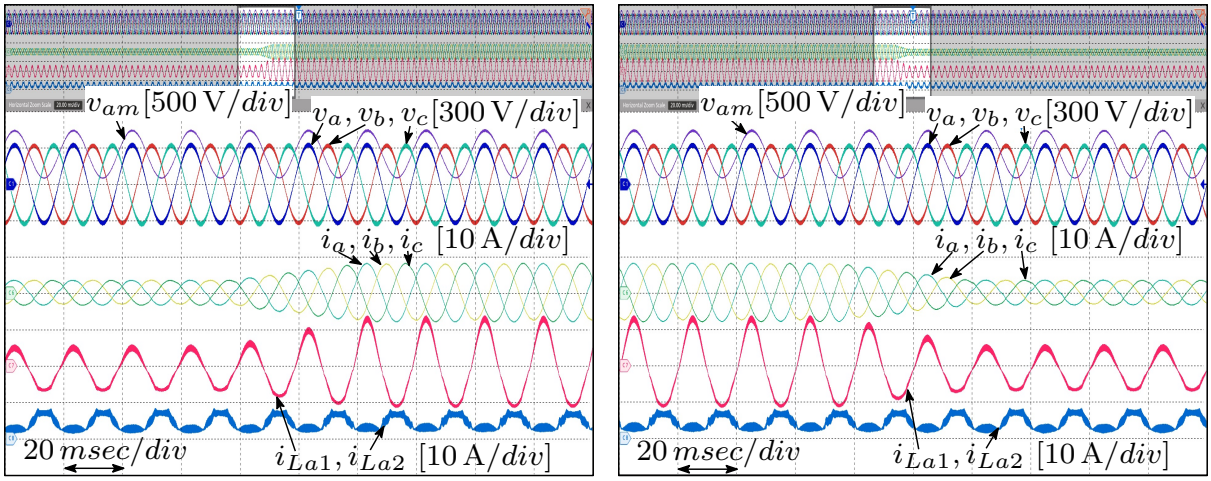


Figure 26: Experimental waveforms illustrating the transient behavior of the proposed converter in Mode I with the clamped $i_{La2_{av}}$ waveform at V_{dc1} equals 400 V, V_{dc2} equals 500 V, and P_{dc1} equals 0.5 kW: (a) P_{dc1} is increased from 1 kW to 3 kW; and (b) P_{dc1} is decreased from 3 kW to 1 kW.

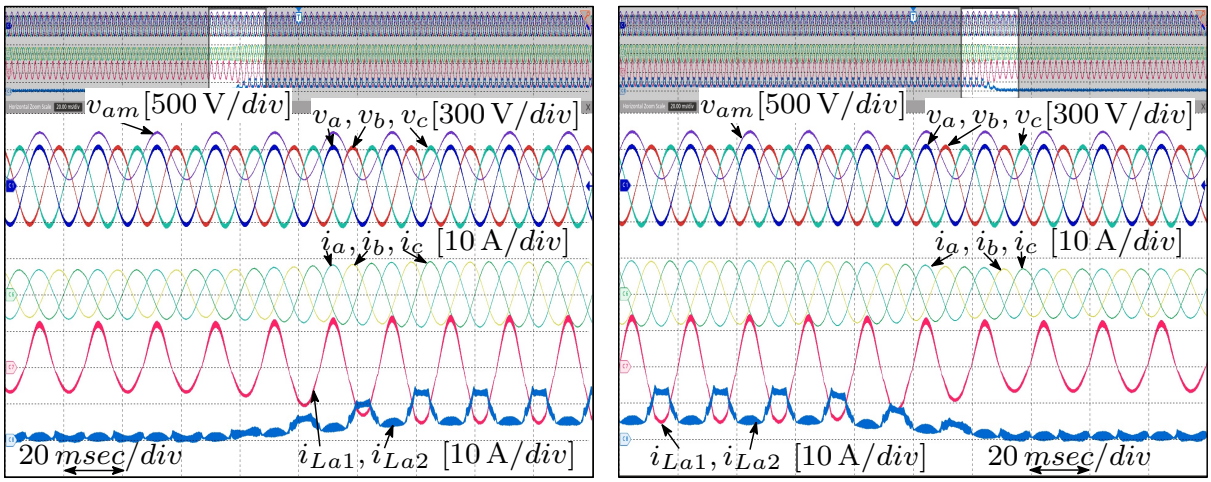


Figure 27: Experimental waveforms illustrating the transient behavior of the proposed converter in Mode I with the clamped $i_{La2_{av}}$ waveform at V_{dc1} equals 400 V, V_{dc2} equals 500 V, and P_{dc1} equals 3 kW: (a) P_{dc2} is increased from 0.1 kW to 1 kW; and (b) P_{dc2} is decreased from 1 kW to 0.1 kW.

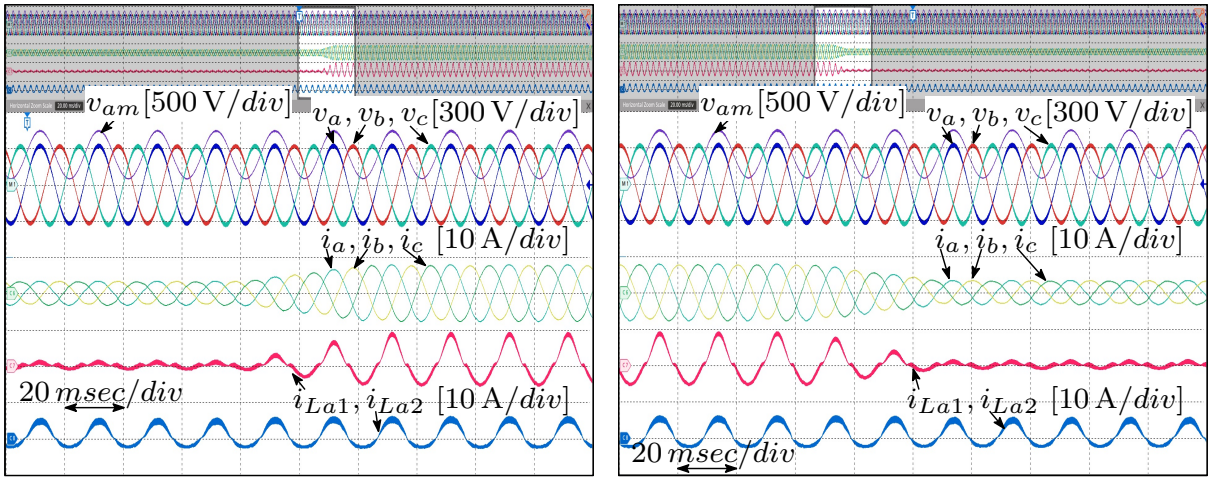


Figure 28: Experimental waveforms illustrating the transient behavior of the proposed converter in Mode II with the original $i_{La2_{av}}$ waveform at V_{dc1} equals 400 V, V_{dc2} equals 500 V, and P_{dc1} equals 0.5 kW: (a) P_{dc1} is increased from 1 kW to 3 kW; and (b) P_{dc1} is decreased from 3 kW to 1 kW.

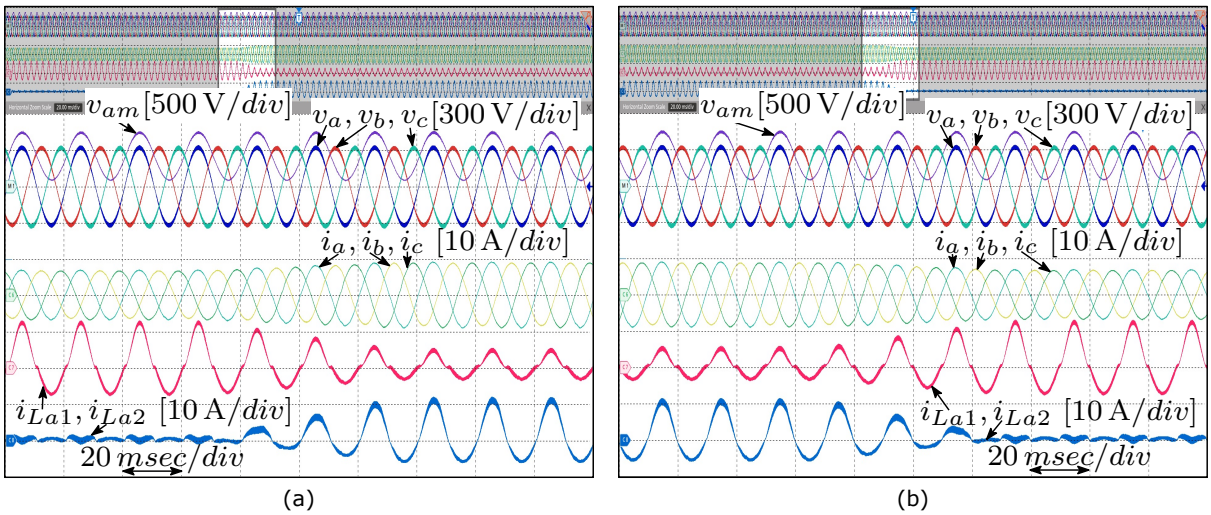


Figure 29: Experimental waveforms illustrating the transient behavior of the proposed converter in Mode I with the original $i_{La2_{av}}$ waveform at V_{dc1} equals 400 V, V_{dc2} equals 500 V, and P_{dc1} equals 3 kW: (a) P_{dc2} is increased from 0.1 kW to 1 kW; and (b) P_{dc2} is decreased from 1 kW to 0.1 kW.

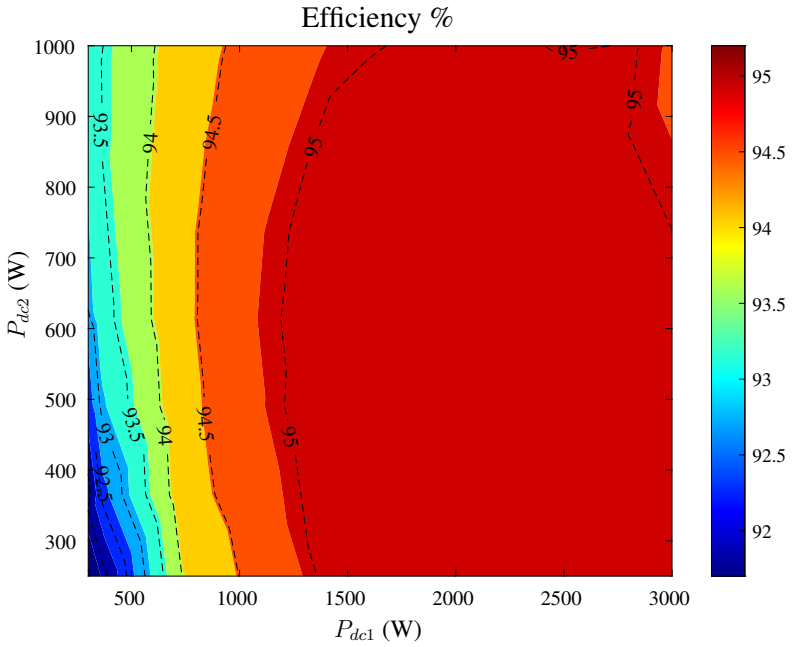


Figure 30: Measured prototype efficiency for different values of P_{dc1} and P_{dc2} when operating in Mode I with the original $i_{La2_{av}}$ waveform at V_{dc1} equals $400\,\text{V}$, V_{dc2} equals $500\,\text{V}$.

4.4.5 Efficiency Evaluation

The prototype efficiency is measured using the Dewesoft SIRIUS XHS high-speed data acquisition system for a wide spectrum of P_{dc1} and P_{dc2}. In the following results, P_{dc1} is swept from $0.3\,\text{kW}$ to $3\,\text{kW}$ with a fixed step of $0.1\,\text{kW}$, and P_{dc2} is swept from $0.25\,\text{kW}$ to $1\,\text{kW}$ with a fixed step of $0.05\,\text{kW}$. The efficiency measurements are reported as a fitted contour plot at different values of P_{dc1} and P_{dc2}.

The efficiency measurements are presented for Mode I with different $i_{La2_{av}}$ waveforms, as well as for Mode II, to provide a comprehensive evaluation of the converter's performance across a variety of operating conditions.

4.4.5.1 Mode I ($V_{dc1} < V_{dc2}$) The efficiency of the prototype is measured when operating in Mode I across different current modes using V_{dc1} of $400\,\text{V}$ and V_{dc2} of $500\,\text{V}$.

In Mode I with the original $i_{La2_{av}}$ waveform, the prototype demonstrated a peak efficiency of 95.36%, achieved at P_{dc1} of $2.1\,\text{kW}$ and P_{dc2} of $0.4\,\text{kW}$, as shown in Fig. 30. At full load, the converter reached an efficiency of 94.89%.

For Mode I with the dc $i_{La2_{av}}$ waveform, the prototype reached a peak efficiency of 95.29% at P_{dc1} of $2.2\,\text{kW}$ and P_{dc2} of $0.3\,\text{kW}$, as illustrated in Fig. 31. At full load, the efficiency was measured at 94.25%.

Finally, when operating in Mode I with the clamped $i_{La2_{av}}$ waveform, the peak efficiency reached 94.88% at P_{dc1} of $2.3\,\text{kW}$ and P_{dc2} of $0.25\,\text{kW}$, as shown in Fig. 32. The full load efficiency for this mode was recorded at 93.59%.

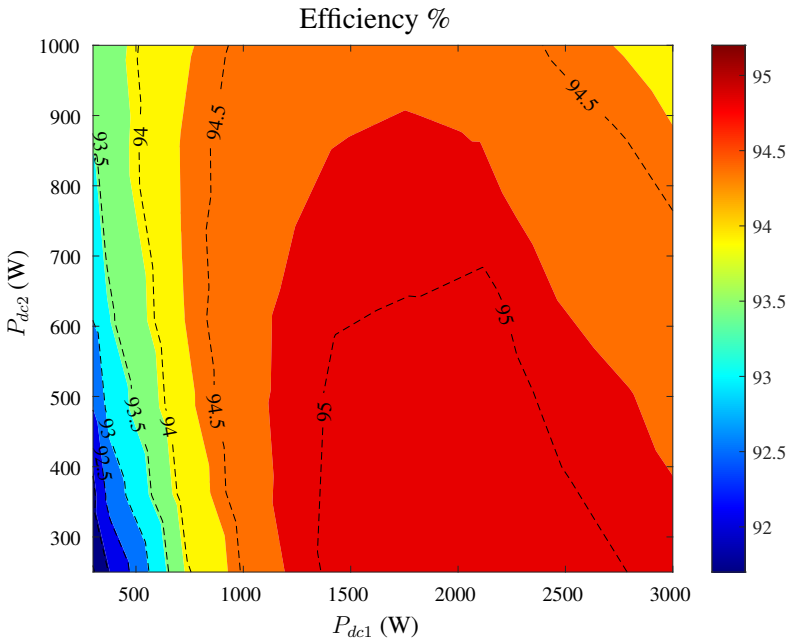


Figure 31: Measured prototype efficiency for different values of P_{dc1} and P_{dc2} when operating in Mode I with the dc $i_{La2_{av}}$ waveform at V_{dc1} equals $400\,\text{V}$, V_{dc2} equals $500\,\text{V}$.

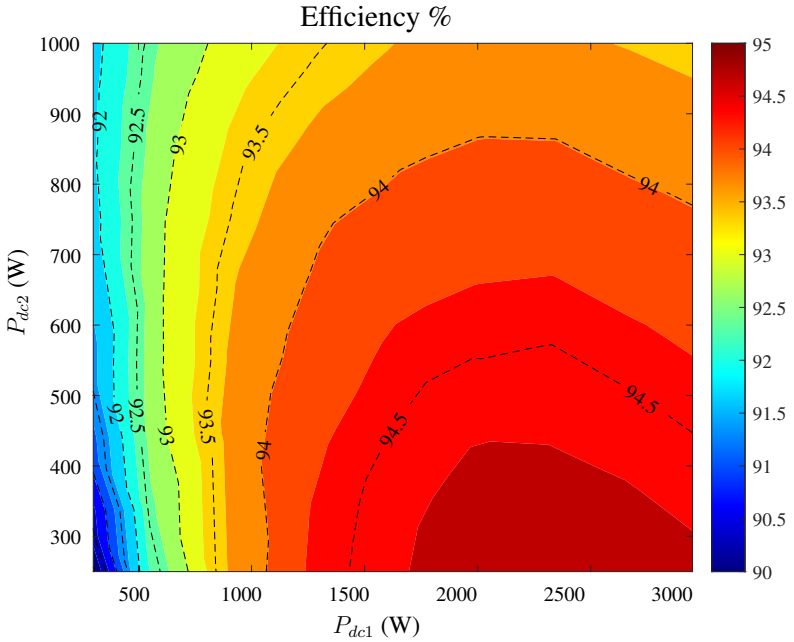


Figure 32: Measured prototype efficiency for different values of P_{dc1} and P_{dc2} when operating in Mode I with the clamped $i_{La2_{av}}$ waveform at V_{dc1} equals $400\,\text{V}$, V_{dc2} equals $500\,\text{V}$.

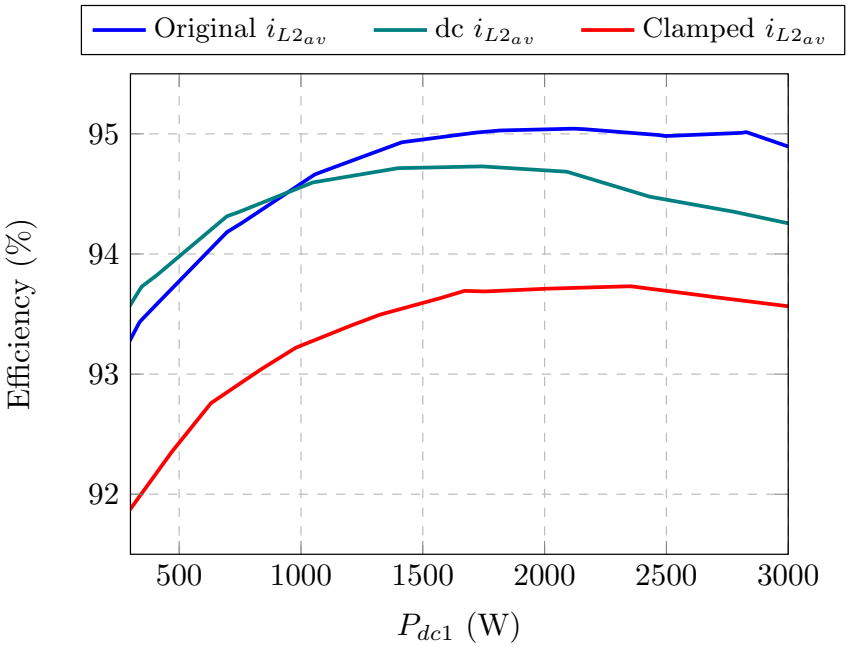


Figure 33: Efficiency comparison of the proposed converter in Mode I with different $i_{L2_{av}}$ wavefroms. The efficiency is evaluated across a range of P_{dc1} values at P_{dc2} equals $1\,$kW, V_{dc1} equals $400\,$V, and V_{dc2} equals $500\,$V.

To better highlight the efficiency performance of the proposed converter across the three $i_{L2_{av}}$ waveforms, Fig. 33 presents the efficiency in Mode I. The efficiency is evaluated across the P_{dc1} range with P_{dc2} equals $1\,$kW, V_{dc1} equals $400\,$V, and V_{dc2} equals $500\,$V.

The results show that the original $i_{L2_{av}}$ waveform achieves the highest efficiency for most of the P_{dc1} range, maintaining a nearly flat efficiency curve for P_{dc1} higher than $1.5\,$kW. The dc $i_{L2_{av}}$ waveform exhibits the highest efficiency at light loads (up to P_{dc1} equals $0.92\,$kW), but closely follows the original $i_{L2_{av}}$ waveform for higher P_{dc1} values, with a slightly lower efficiency. Lastly, the clamped $i_{L2_{av}}$ waveform consistently demonstrates the lowest efficiency across the full P_{dc1} range.

Additionally, Fig. 34 presents the efficiency in Mode I across the P_{dc2} range, with P_{dc1} set to $3\,$kW, V_{dc1} set to $400\,$V, and V_{dc2} set to $500\,$V. Once again, the results demonstrate that the original $i_{L2_{av}}$ waveform achieves the highest efficiency throughout the entire P_{dc2} range, maintaining a nearly flat efficiency curve.

In contrast, the dc $i_{L2_{av}}$ waveform exhibits a lower efficiency compared to the original waveform, with efficiency decreasing from 94.92% at P_{dc2} of $0.25\,$kW to 94.25% at P_{dc2} of $1\,$kW. Lastly, the clamped $i_{L2_{av}}$ waveform consistently shows the lowest efficiency across the entire P_{dc2} range, with a drop in efficiency from 94.77% at P_{dc2} of $0.25\,$kW to 93.57% at P_{dc2} of $1\,$kW.

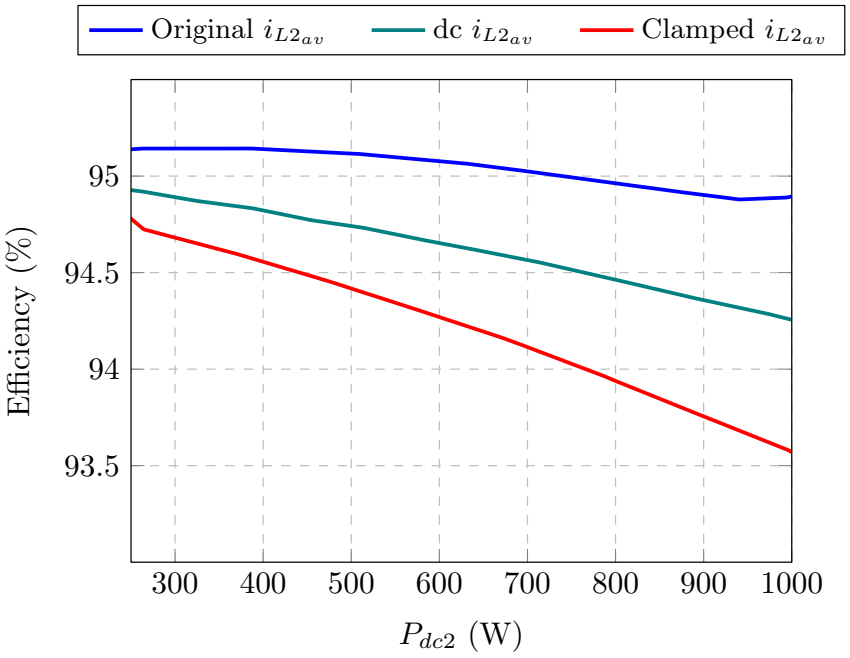


Figure 34: Efficiency comparison of the proposed converter in Mode I with different $i_{L2_{av}}$ wavefroms. The efficiency is evaluated across a range of P_{dc2} values at P_{dc1} equals $3\,$kW, V_{dc1} equals $400\,$V, and V_{dc2} equals $500\,$V.

4.4.5.2 Mode II ($V_{dc1} < V_{dc2}$) The efficiency of the prototype when operating in Mode II with the original $i_{La2_{av}}$ waveform, at $V_{dc1} = 500\,$V and $V_{dc2} = 400\,$V, is reported in Fig. 35. In this mode, the prototype demonstrates a peak efficiency of 96.04% at at P_{dc1} and P_{dc2} equal to $2.3\,$kW and $0.6\,$kW, respectively. Additionally, the converter achieves an efficiency of 95.68% at full load.

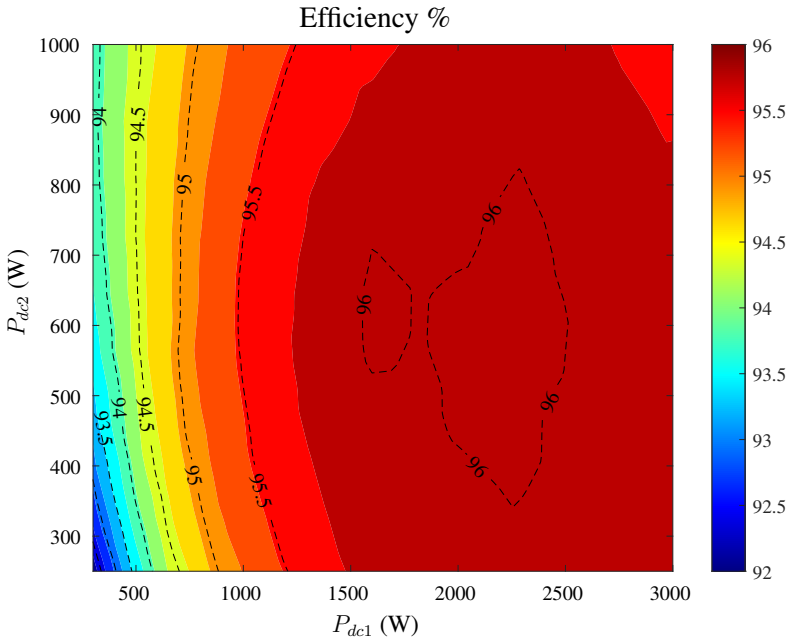


Figure 35: Measured prototype efficiency for different values of P_{dc1} and P_{dc2} when operating in Mode II with the original $i_{La2_{av}}$ waveform at V_{dc1} equals $500\,\text{V}$, V_{dc2} equals $400\,\text{V}$.

4.5 Conclusion

This section introduces the Asymmetric Multiport Y-converter, a single-stage non-isolated multiport converter for interfacing the three-phase ac grid with dc systems. Compared to the Multiport Y-converter, the Asymmetric Multiport Y-converter features a simplified structure with fewer semiconductor devices and inductors, while maintaining the same key capabilities, such as single-stage power conversion across multiple ports, buck-boost functionality, and bidirectional power flow at all ports. Challenges associated with the Asymmetric Multiport Y-converter, such as maintaining balanced ac grid currents due to its asymmetric structure and minimizing low-frequency voltage ripples at the dc ports, are addressed with proposed solutions. The performance of the converter is validated through experimental tests under various operating conditions, including steady-state, transient results, and efficiency evaluations.

5 Performance Evaluation of Multiport Y-Converters using Renewable Source Mission Profile

5.1 Introduction

The rise of renewable energy is reshaping electrical grids, driven particularly by the increased adoption of distributed energy resources (DERs). Current efforts in the energy sector, led by researchers and policymakers, are focused on creating effective solutions to transition from traditional fossil-fuel-based power systems to green energy systems [18]. While traditional network reinforcement remains a viable option for increasing grid capacity, it presents critical drawbacks, such as high costs and long implementation times. In contrast, dc microgrids (MGs) have emerged as an effective solution for addressing local energy needs. These systems integrate distributed power sources directly into distribution networks and are highly compatible with renewable energy sources, modern electric loads, and energy storage systems [19].

As the adoption of dc MGs continues to grow, there is an increasing need to re-evaluate how these systems are efficiently interfaced with existing ac grids. Achieving high efficiency, compactness, and scalability is essential—especially as the number of interconnected dc MGs expands. Two main design strategies are considered, as illustrated in Fig. 36: deploying multiple two-port converters, each dedicated to a single dc MG, or utilizing a single multiport converter capable of simultaneously interfacing multiple dc MGs.

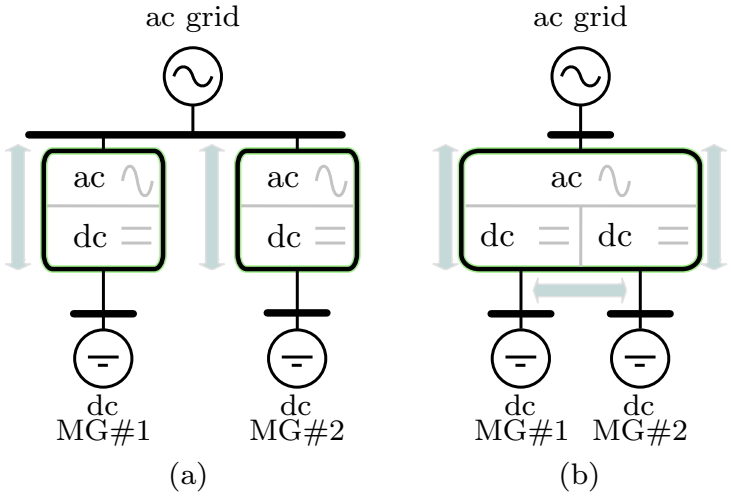


Figure 36: ac grid integration of two dc MGs: (a) separate two-port converters vs. (b) multiport converter.

Given the motivations for adopting 400 V as the voltage level for residential dc MGs [20], this study focuses on interfacing a 400 V dc MG with the European low-voltage ac grid, which also operates at a 400 V line-to-line voltage. Buck-type rectifiers are particularly

well-suited for this application, as they can directly step down the ac voltage to the dc level [21]. In contrast, boost-type converters—such as the two-level voltage source converter (VSC)—require an additional buck stage, increasing system complexity and reducing overall efficiency.

Among the various buck-type topologies reported in the literature, the Y-converter has demonstrated superior performance, as highlighted in [22], compared to other state-of-the-art solutions such as current source converters (CSCs) in both six-switch and seven-switch configurations [23, 24], as well as the Swiss converter [25]. The key advantages of the Y-converter include single-stage power conversion, bidirectional power flow, and buck-boost capability, which enables flexible energy transfer between the ac and dc sides. These features enhance its versatility across a wide range of applications.

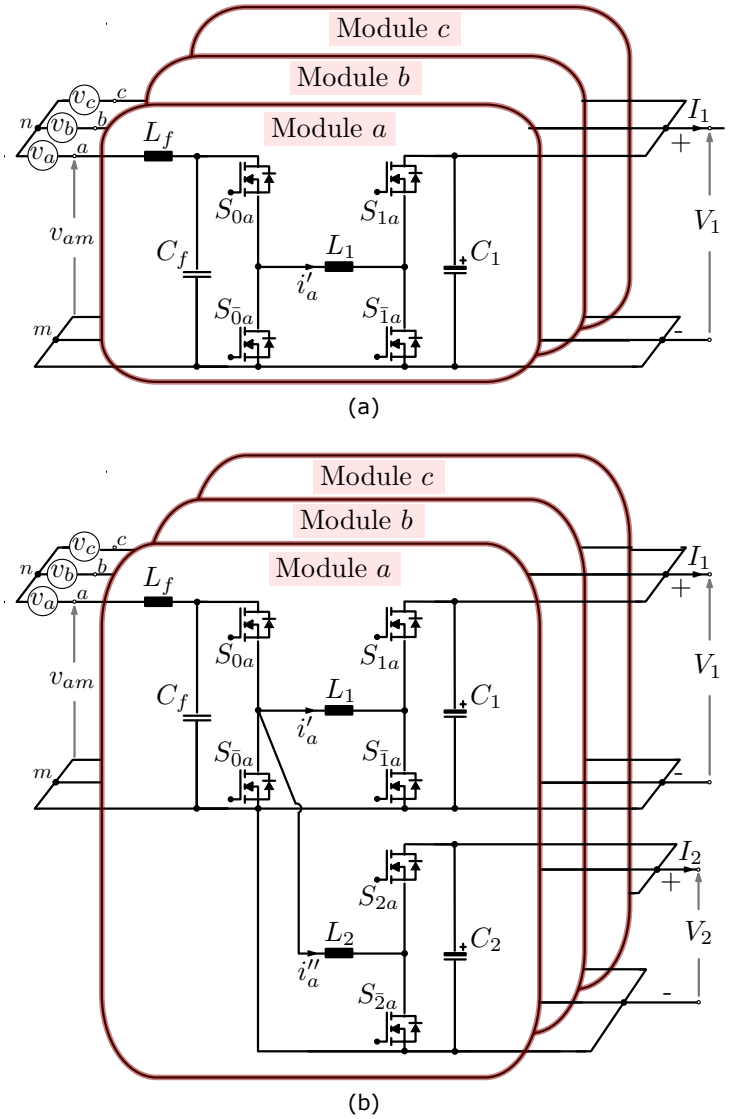
Building on this foundation, the multiport structure, introduced in [26], extends the basic two-port Y-converter by incorporating additional dc ports. This advancement allows for the simultaneous integration of multiple dc sources and loads, significantly improving system-level flexibility and energy management. The topological schematics of the Y-converter and its multiport extension are illustrated in Fig. 37a and Fig. 37b, respectively.

Previous studies [22, 26] have demonstrated that the Y-converter and its multiport variant offer efficient integration of dc energy resources and effective energy management within dc MGs, while ensuring seamless interfacing with the ac grid.

This research focuses on optimizing a power electronic interface that connects two dc ports and one ac port. The main objectives are to achieve high efficiency—minimizing energy losses and operational costs—and to maximize power density for a compact design. Two design approaches are investigated and compared: the first utilizes a single multiport Y-converter, which consolidates multiple energy pathways into a unified converter unit; the second employs a dual Y-converter configuration, in which two independent Y-converters are used to achieve the same functionality.

The performance of both configurations is evaluated in terms of efficiency and power density under two application scenarios. The first scenario considers the interconnection of two 400 V dc MGs, where the nominal efficiency is assessed under full power operation at each port. The second scenario focuses on renewable energy integration, with a photovoltaic (PV) system connected to the first dc port and an energy storage system to the second. Here, the average efficiency is calculated over a realistic PV mission profile to evaluate energy conversion performance under variable operating conditions.

The remainder of the section is structured as follows: Sec. 5.2 describes the multi-objective optimization (MOO) procedure, including component modeling and key design trade-offs. Sec. 5.3 outlines the methodology for mission-profile-based efficiency evaluation under dynamic renewable energy conditions. Sec. 5.4 presents a comparative analysis



(a)

(b)

Figure 37: Schematics of the evaluated topologies: (a) two port Y-converter; (b) multiport Y-converter (MPC).

of the results, focusing on efficiency, power density, and component-level losses and volume for both the MPC and 2Y configurations. Finally, Sec. 5.5 concludes the study and summarizes key findings.

5.2 Multi-Objective Optimization Procedure

The MOO provides a framework for systematically exploring inherent trade-offs in complex systems, such as power electronics converters, where competing performance metrics cannot be simultaneously optimized [27]. For example, increasing switching frequency (f_{sw}) may improve power density (reducing component size) but degrade efficiency due to higher switching and inductor losses. Traditional single-objective optimization risks suboptimal outcomes by prioritizing one performance metric at the expense of others. In

contrast, MOO identifies Pareto-optimal solution designs where no further improvement can be achieved in one objective without affecting another, thereby preserving balance across performance indices [28].

This work employs MOO to design the power electronics converters under study. A flowchart of the MOO methodology highlighting design space exploration and Pareto front generation is presented in Fig. 38. The flowchart covers tunable parameters, component selections, and practical constraints. Efficiency and power density are selected as critical performance indices: efficiency governs energy savings, while power density determines compactness, a key driver in modern energy systems. Using the direct-search method, we generate the Pareto front (i.e., the set of non-dominated design solutions representing optimal compromises) between efficiency and power density.

The MOO procedure begins by defining the system specifications, including power ratings, voltage levels, and design constraints. Next, the modulation scheme, material datasets, and sweep parameters are selected. A comprehensive exploration of the design space is then carried out by varying tunable parameters and component choices. Each design iteration is evaluated to assess its impact on efficiency and power density—the two primary objectives used to identify the Pareto-optimal trade-off.

5.2.1 Component Modeling

Component modeling which is critical to the optimization framework is summarized below.

5.2.1.1 Semiconductor Design The semiconductor loss model integrates time-varying current and voltage waveforms derived from steady-state analysis under the selected modulation. Conduction losses are computed as functions of the instantaneous current, average junction temperature (T_j), and temperature-dependent on-state resistance. Switching losses (E_{on}, E_{off}) are calculated using waveform data and experimentally obtained loss maps [29]. These losses feed into a thermal network model to iteratively compute T_j, accounting for junction-to-ambient thermal resistance and heatsink performance. This iterative coupling ensures accurate loss-volume trade-offs for semiconductors and heatsinks.

5.2.1.2 Inductor Design The magnetic design methodology begins with a reluctance-based model that accounts for core nonlinearities, such as flux-dependent permeability, and air gap effects. Core losses are estimated using the improved-improved generalized Steinmetz equation (i^{2}GSE, [30]), with operating-point-dependent Steinmetz coefficients extracted from experimentally derived loss maps. Winding losses are computed by accounting for both skin and proximity effects, with copper conductivity corrected for temperature variations. Finally, a thermal model is applied to predict the inductor's internal temperature distribution [31].

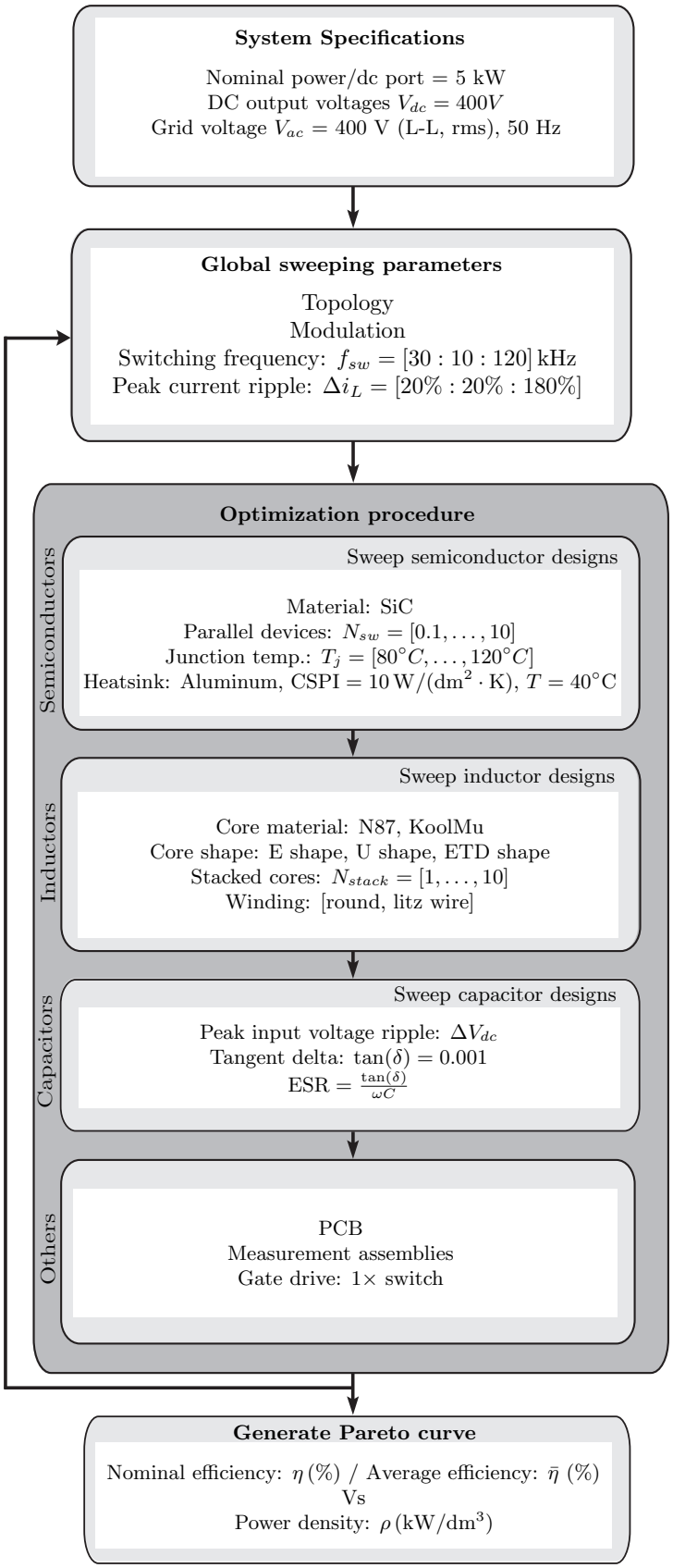


Figure 38: Flowchart of the MOO methodology highlighting design space exploration and Pareto front generation.

5.2.1.3 Capacitor Design Capacitor designs are evaluated based on their losses, modeled via frequency- and temperature-dependent equivalent series resistance (ESR). The design space includes capacitor type (e.g., film, ceramic), rated capacitance, and voltage, enabling exploration of size-loss compromises.

5.3 Mission-Profile Efficiency Calculation Methodology

This section presents a methodology for computing the average efficiency of the multiport converter under a realistic photovoltaic mission profile, while maintaining low computational effort. The first step involves precomputing the converter's power-dependent losses at discrete operating points for Port-1 (P_{dc1}) and Port-2 (P_{dc2}). These points cover bidirectional power levels relative to each port's rated power ($P_{\text{dc,rated1}}$, $P_{\text{dc,rated2}}$):

$$\{P_{\text{dc1}}\} = \left\{-P_{\text{dc,rated1}}, -\left(P_{\text{dc,rated1}} - \Delta P_1\right), \ldots, P_{\text{dc,rated1}}\right\} \tag{26}$$

$$\{P_{\text{dc2}}\} = \left\{-P_{\text{dc,rated2}}, -\left(P_{\text{dc,rated2}} - \Delta P_2\right), \ldots, P_{\text{dc,rated2}}\right\} \tag{27}$$

where

$$\Delta P_1 = \frac{2P_{\text{dc,rated1}}}{N}, \quad \Delta P_2 = \frac{2P_{\text{dc,rated2}}}{M} \tag{28}$$

define the step sizes for N and M grid points. For instance, a 10-point grid for a 5 kW port yields: $-5, -4, \ldots, 5$ kW. The resulting loss matrix Γ of dimensions $N \times M$ maps each $(P_{\text{dc1}}, P_{\text{dc2}})$ combination to its corresponding loss value. The 250-hour PV power profile shown in Fig. 40b, $P_{\text{PV}}(t)$, is used to compute the converter losses at each point of the PV profile. The ac port power P_{ac} is fixed as the time-averaged PV power:

$$P_{\text{ac}} = \frac{1}{250} \sum_{t=0}^{250} P_{\text{PV}}(t) \tag{29}$$

The storage port dynamically balances the system to ensures that the storage absorbs PV variability, maintaining constant P_{ac} despite fluctuating PV input, yielding

$$P_{\text{storage}}(t) = P_{\text{PV}}(t) - P_{\text{ac}} \tag{30}$$

For each timestep t, the converter's instantaneous loss $\Gamma(t)$ is estimated using a two-dimensional interpolation method over the precomputed loss surface Γ at the corresponding operating points $(P_{\text{dc1}}, P_{\text{dc2}})$:

$$\Gamma(t) = \Gamma(P_{\text{dc1}} = P_{\text{PV}}(t), P_{\text{dc2}} = P_{\text{storage}}(t)) \tag{31}$$

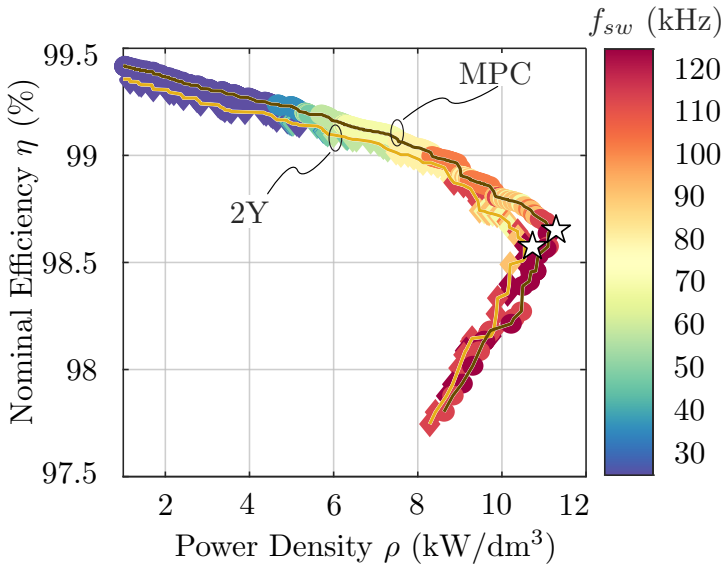


Figure 39: Pareto-front evaluation of both designs considering nominal efficiency.

To evaluate average efficiency, the instantaneous operating power $P_{\mathsf{op}}(t)$ is also defined as:

$$P_{\mathsf{op}}(t) = \max\left(|P_{\mathsf{PV}}(t)|, |P_{\mathsf{storage}}(t)|, |P_{\mathsf{ac}}|\right) \tag{32}$$

The average efficiency η_{avg} is then computed over the evaluated time span as:

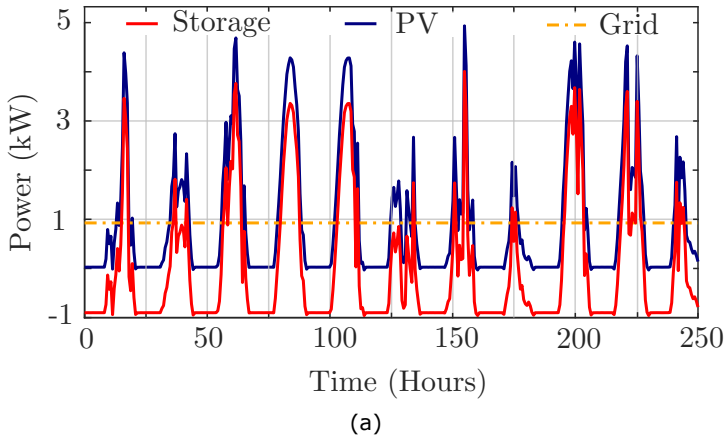
$$\eta_{\mathsf{avg}} = \frac{\sum_{t=0}^{250} P_{\mathsf{op}}(t)}{\sum_{t=0}^{250} P_{\mathsf{op}}(t) + \sum_{t=0}^{250} \Gamma(t)} \times 100\% \tag{33}$$

5.4 Results and Discussion

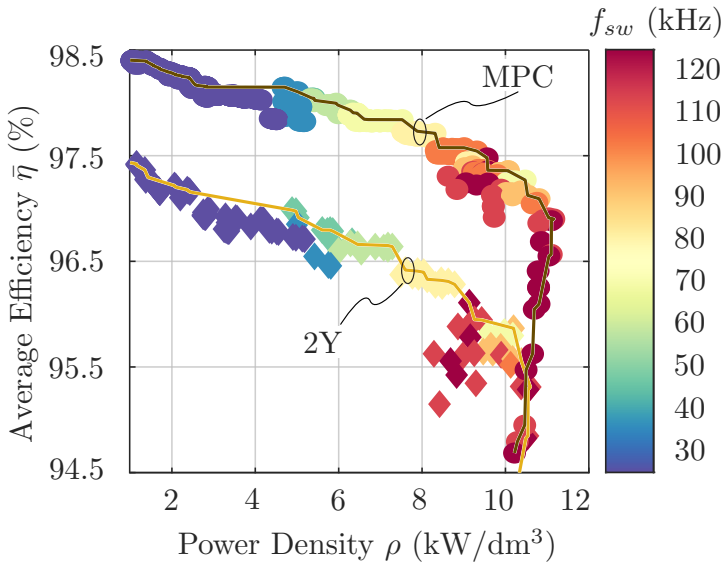
Fig. 39 presents the η-ρ Pareto front for the investigated designs in case of dc MGs interconnection at nominal power conditions for each ports. The results highlight that low-frequency designs exhibit reduced power density due to the increased volume of magnetic components, whereas higher-frequency designs lead to lower efficiency. This behavior is consistent for both the MPC and the 2Y configurations. Both configurations achieve efficiencies exceeding 97.5% across the evaluated range, with peak efficiencies surpassing 98.5% at the maximum power-density points. Notably, the MPC demonstrates a slight advantage over the 2Y configuration, achieving higher power density for a given efficiency.

Fig. 40a illustrates the mission profile, where a PV system is connected to dc port 1 and a storage system to dc port 2, while constant ac power is supplied to the grid. The resulting average efficiencies of both configurations under this profile are shown in Fig. 40b. Even if both configurations achieve high efficiency, the MPC achieves an average efficiency of 96.8%, compared to 95.3% for the 2Y configuration at the power density limit—an

improvement of 1.5%. This gain is primarily attributed to the MPC's capability to directly transfer power between dc ports, thereby reducing semiconductor losses in the ac stage. In contrast, the 2Y configuration incurs additional losses in the ac stage even during dc-dc power transfers.



(a)



(b)

Figure 40: Mission-profile based evaluation of both configurations: (a) The Mission profile adopted in the evaluation; (b) Pareto-front evaluation of both designs considering average efficiency.

The maximum power-density points of the MPC and 2Y designs in Fig. 39 were chosen to conduct a detailed volume and loss breakdown analysis. Fig. 41a illustrates the volume distribution, where ac capacitors dominate (31.5% for MPC and 36.6% for 2Y), followed by inductors (31.1% for MPC and 21.8% for 2Y) and semiconductor components. The ac-line filter's inductors are not included in the comparison between the MPC and 2Y design concepts.

At the same time, Fig. 41b breaks down losses for both designs, revealing lower total losses in the MPC. The primary contributors are core and copper losses in inductors,

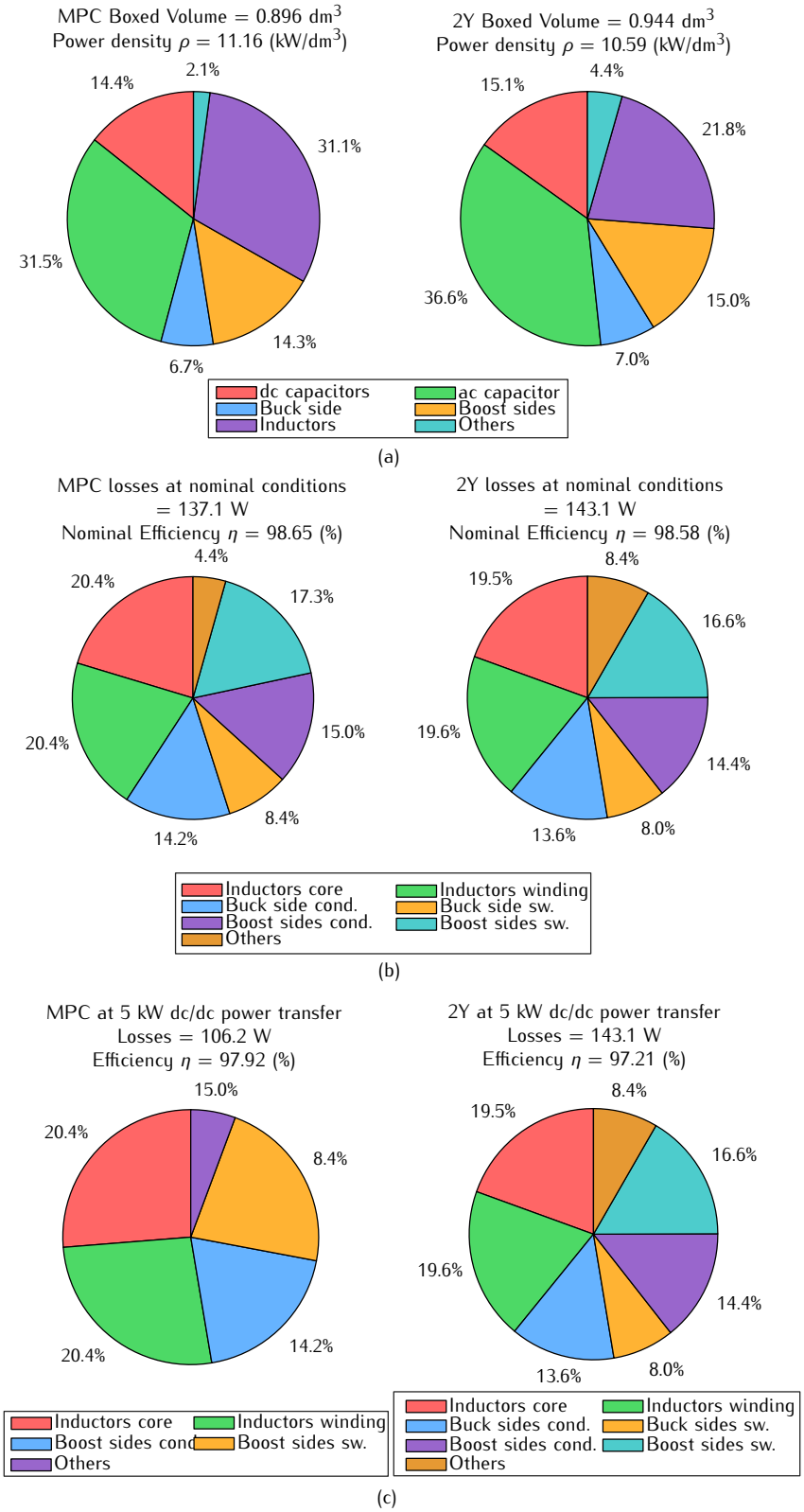


Figure 41: (a) Components' volume distribution at the maximum power-density points. (b) Power loss distribution across converter components at the maximum power-density points. (c) dc-dc power transfer loss comparison between MPC and 2Y topologies

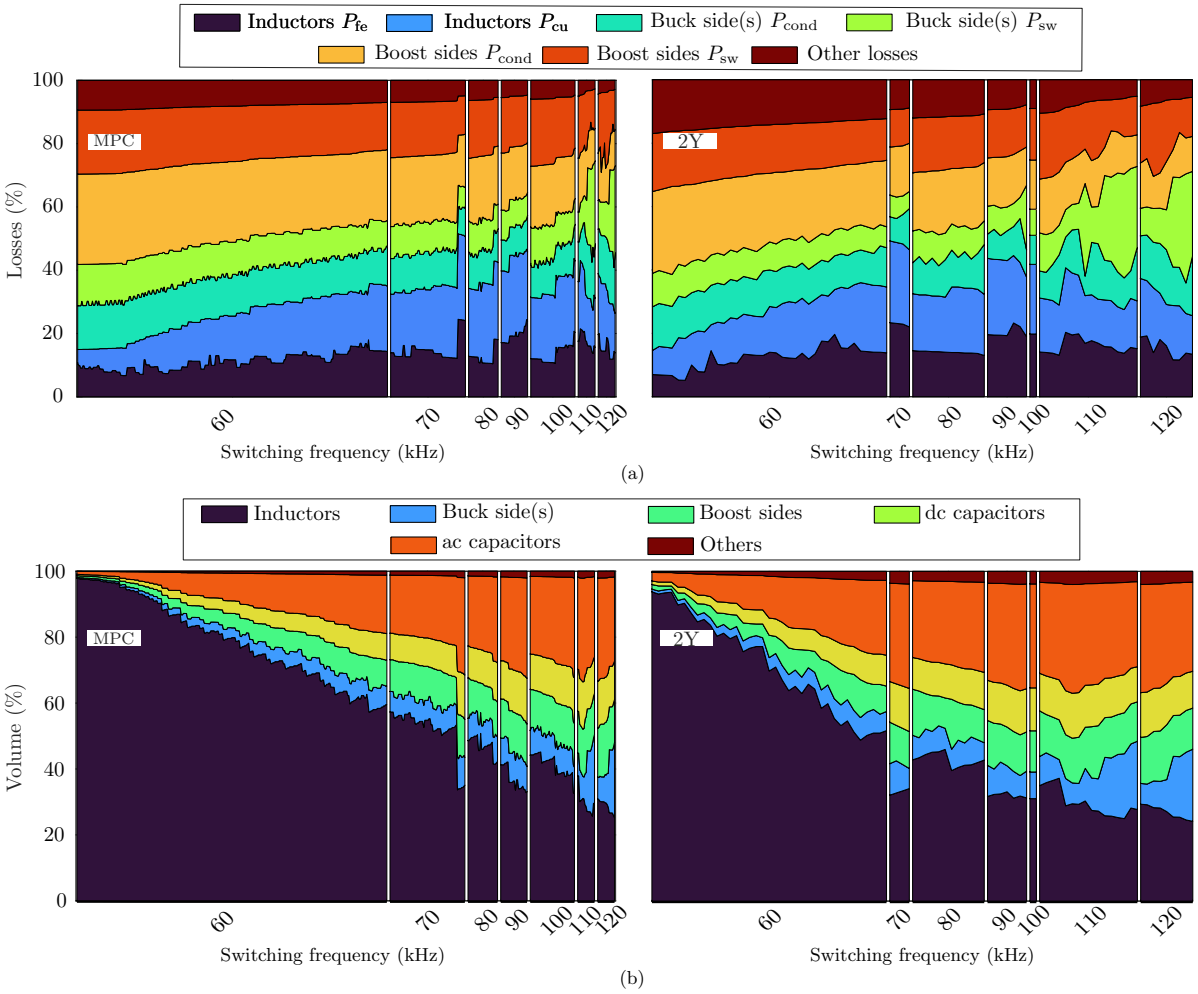


Figure 42: Distribution of (a) losses and (b) volume for the evaluated converter designs.

followed by conduction losses in boost-side semiconductors and buck-side semiconductor losses. Fig. 41c analyzes the designs under dc-dc power transfer conditions, with corresponding losses detailed. The MPC design concept enables direct dc-dc power transfer, eliminating ac-side losses and achieving total losses of 106.2 W. In contrast, the 2Y design lacks a direct dc path, incurring additional buck-side semiconductor losses resulting in a total losses of 143.1 W, a 34.7% increase compared to the MPC. This difference highlights the efficiency benefit of direct power transfer in the MPC.

Fig. 42 shows the loss and volume distribution for the Pareto-optimal design solutions generated by the MOO presented in Fig. 39, in which the trade-off between nominal efficiency and power density is shown as a Pareto front and each point along the curves represents an optimized design found for a specific switching frequency, which is color defined. Fig. 42 further details the internal component-wise distribution of losses and volume for these designs at their respective operating frequencies. Fig. 42a show the percentage distribution of power losses among components for the pareto front MPC and 2Y converter

designs, respectively, as a function of switching frequency. The x-axis spans from 60 kHz to 120 kHz. For each frequency, the plots shows on y-axis the percentage share of each component's loss to the total power loss in the corresponding optimized design.

The stacked areas indicate that at lower frequencies, dominant losses results from inductor iron losses (P_{fe}), copper losses (P_{cu}), and semiconductor conduction losses (P_{cond}). As the switching frequency increases, the percentage contribution from semiconductor switching losses (P_{sw}), in both buck and boost stages, increase.

Fig. 42b shows the percentage distribution of volume among components for the pareto front MPC and 2Y designs across the switching frequency range of 60 kHz to 120 kHz. The x-axis represents the switching frequency, while the y-axis represents each component's share of the total volume for the corresponding optimized design.

The stacked areas shows that, at lower frequencies, inductors occupy the largest share of volume. As the frequency increases, the volume share of inductors decreases sharply. In contrast, other components such as semiconductors, buck and boost sides' elements (including heatsinks), and both dc and ac capacitors contribute a larger percentage to the total volume.

5.5 Conclusion

This research highlights the optimization of multiport Y-converter solutions to interface two dc ports and an ac port using a single converter. By focusing on the Y-converter and its multiport extension, the study demonstrates the potential of these topologies to achieve high efficiency and power density.

The multiport Y-converter and the two separate Y-converter configuration were systematically analyzed using a multi-objective optimization framework. The results reveal that both configurations can achieve knee solutions with efficiencies exceeding 98.5% at power densities higher than 10 kW/dm³. However, the MPC exhibits better performance in terms of power density for a given efficiency. Furthermore, the MPC demonstrated enhanced average efficiency performance during power transfer between dc ports due to the elimination of losses on the ac side.

6 Nonlinear Control of the Y-Converters for Grid Integration of 400 V DC Microgrids

6.1 Introduction

The evolution of modern power systems is increasingly oriented toward hybrid configurations, where traditional ac grids operate alongside advanced dc microgrids (MGs) [32, 33]. Integrating ac and dc networks enhances power exchange efficiency between conventional infrastructure and energy-efficient dc systems [34, 35]. At the core of this interaction are power factor correction (PFC) converters, which ensure reliable and efficient power transfer between the two domains while maintaining power quality and meeting the stringent operational requirements of hybrid networks [36].

In low-voltage (LV) dc MGs, the 400 V dc system has emerged as the preferred choice for residential and commercial applications [37] due to its superior overall efficiency and reduced number of power conversion stages. When interfacing with the low-voltage (LV) European ac grid, buck-type converters are typically employed for single-stage power conversion, whereas boost-type converters require an additional back-end buck stage. Among the various topologies explored in the literature, the Four-Wire (4-W) Y-converter has demonstrated superior performance [38]. Unlike conventional buck-type converters, the 4-W configuration offers enhanced control under unbalanced conditions, improved fault tolerance, and the capability to operate in islanded mode, supporting both single-phase and three-phase loads. Compared to traditional boost-type converters, the 4-W Y-converter eliminates the need for two-stage conversion, thereby enhancing efficiency and power density. Additionally, it enables grounding of both the ac grid and the unipolar dc MG without requiring isolation.

The structure of the Y-converter, shown in Fig. 43, presents challenges for its control as a power factor correction (PFC) converter. Each module of the Four-Wire (4-W) Y-converter operates as a four-switch buck-boost converter with two distinct modes: buck mode, when the ac-side module voltage exceeds the dc-side voltage, and boost mode otherwise. This hybrid operation complicates the design of linear controllers, as their performance must be optimized for both modes. Additionally, grid current control in various Y-converter structures relies on indirect measurements of the ac grid currents [39, 40], where the grid currents are estimated using the inductor currents and the reference duty cycle of the buck half-bridges. While this approach simplifies the control structure, deviations between the reference and actual duty cycle can introduce distortions in the grid currents.

In this section, a unity-power-factor control strategy based on the synthesis of a loss-free resistor (LFR) [41] using sliding-mode control (SMC) [42] is proposed for the four-

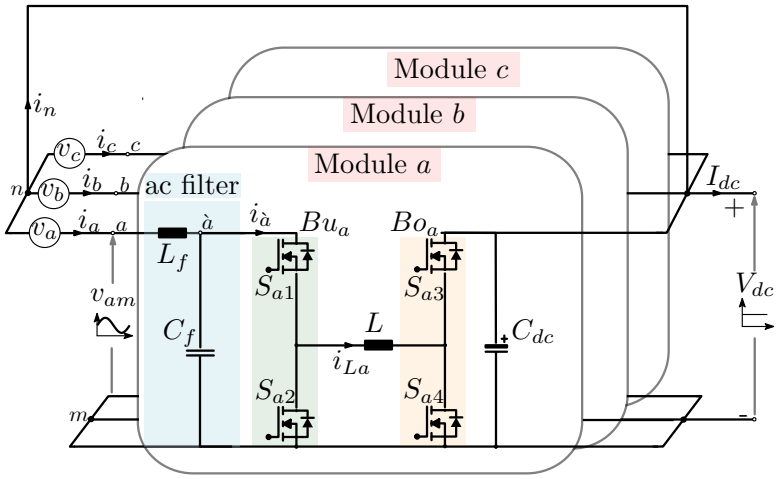


Figure 43: Schematic of the four-wire Y-converter.

wire Y-converter to address the limitations of conventional linear controllers. The proposed control strategy overcomes the limitations of conventional controllers by improving dynamic performance through real-time switching actions. Real-time switching actions refer to the direct generation of gate signals based on instantaneous system measurements, eliminating the need for modulation or averaging steps and thereby enabling faster and more responsive control. This approach ensures precise regulation of current and voltage with minimal delay, enabling fast power balancing within the dc MG [43, 44]. Moreover, the implementation of LFR synthesis streamlines the control structure, particularly under unbalanced ac grid conditions, where the emulated LFR of each phase can be controlled independently to enable enhanced flexability in regulation. The rest of the paper is structured as follows: Sec. 6.2 discusses the principles of converter operation and the proposed controller; Sec. 6.3 reports the simulation results; and Sec. 6.6 presents the conclusion.

6.2 Analysis of the Y-Converter as loss-free resistor in sliding-mode control

The 4-W Y-converter, shown in Fig. 43, consists of three buck-boost modules connected in a star configuration at a central point denoted as (m), while the ac grid neutral (n) is directly connected to the positive rail of the dc side. This direct connection imposes a fixed offset voltage equal to the dc-side voltage V_{dc} on the ac-side voltages v_{am}, v_{bm}, and v_{cm}. Consequently, the ac-side voltage can be expressed as:

$$v_{xm} = v_x + v_{nm} = \hat{V}_m \sin(\omega t + \theta_x) + V_{dc} \tag{34}$$

where v_x, with $x = (a, b, c)$, represents the ac grid phase voltages, $\hat{V}_m$ is the peak phase voltage, ω is the ac grid frequency in rad/s, and θ_x are the respective phase angles of v_x, given by $\theta_x = [0, \pm 2/3\pi]$.

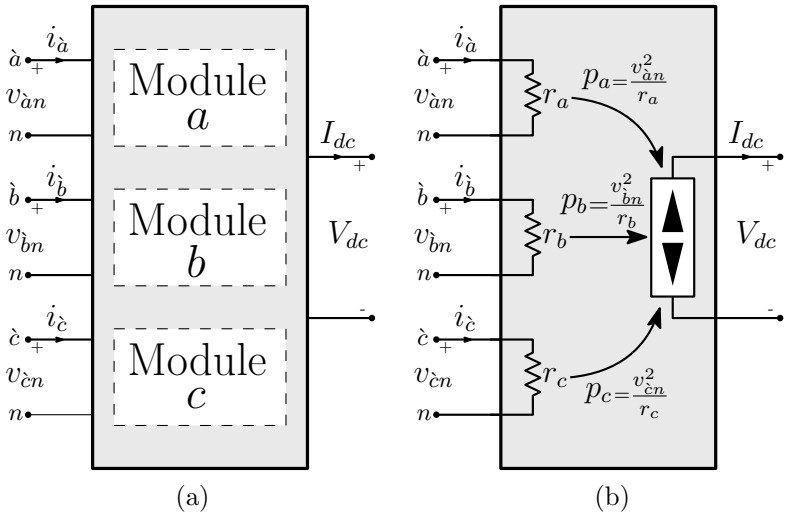


Figure 44: The Four-wire Y-converter emulated as loss-free resistors: a) Tetra-port circuit; b) Loss-free resistor circuits with highlighting the instantaneous power transferred from each phase to the dc MG

Since each module of the Y-converter operates as a dc-dc converter, it is essential to ensure that v_{xm} remains non-negative. Consequently, when interfacing a European low-voltage ac grid with a dc system, V_{dc} must exceed $\hat{V}_m$ (i.e., 325 V). This requirement enables the converter to directly interface with 400 V dc MGs. In the event of a black-start condition in the dc MG, start-up resistors must be employed on the ac grid side to limit the current until V_{dc} exceeds $\hat{V}_m$.

The concept of LFR is based on modeling each module of the 4-W Y-converter as a Power Output Equals Power Input (POPI) circuit. Consequently, the 4-W Y-converter, excluding the input filter, can be represented as a tetra-port circuit, as shown in Fig. 44. SMC is employed to enforce LFR behavior in the Y-converter by emulating each module as a resistance relative to its respective input phase voltage, as illustrated in Fig. 44. Under this assumption, all the power absorbed by these resistances is transmitted to the output port without losses, leading to the following power balance equation:

$$P_{ac} = P_a + P_b + P_c = P_{dc} \tag{35}$$

For a balanced ac grid, the power delivered by each module is given by:

$$P_a = P_b = P_c = \frac{P_{dc}}{3} \tag{36}$$

Consequently, the emulated input resistance of each module, r_x, is expressed as:

$$r_x = \frac{3V_{\text{RMS}}^2}{P_{dc}} \tag{37}$$

where V_{RMS} denotes the RMS value of the phase voltage.

Under unbalanced ac grid conditions, r_x can be controlled independently, offering enhanced flexibility in regulation. Three distinct control modes are considered in such scenarios: constant input current mode, constant input resistance mode, and constant input power mode [45]. The constant input current mode ensures an even distribution of current among the modules, regardless of the grid voltage variations across phases. This leads to nearly equalized current stress on the semiconductor devices and eliminates current flow through the neutral wire. In this mode, the emulated input resistances can be calculated by:

$$\frac{r_a}{V_{\text{RMS}a}} = \frac{r_b}{V_{\text{RMS}b}} = \frac{r_c}{V_{\text{RMS}c}} = \frac{V_{\text{RMS}a} + V_{\text{RMS}b} + V_{\text{RMS}c}}{P_{dc}} \tag{38}$$

In the constant input resistance mode, a fixed emulated resistance is applied to each module, resulting in a current drawn that is proportional to the voltage of each phase. This mode helps restore balanced conditions by drawing less current from the weaker phases with lower voltages, while drawing higher current from the stronger phases. The emulated input resistances in this mode are given by:

$$r_a = r_b = r_c = \frac{V_{\text{RMS}a}^2 + V_{\text{RMS}b}^2 + V_{\text{RMS}c}^2}{P_{dc}} \tag{39}$$

The constant input power mode ensures equalized power sharing among modules, causing the current drawn from each phase to be inversely proportional to its corresponding grid voltage. The emulated input resistances can be determined in this mode as follows:

$$r_a = \frac{3V_{\text{RMS}a}^2}{P_{dc}},\ r_b = \frac{3V_{\text{RMS}b}^2}{P_{dc}},\ r_c = \frac{3V_{\text{RMS}c}^2}{P_{dc}} \tag{40}$$

While (40) can be applied to unbalanced voltages with symmetrical phase angles to suppress power fluctuations at the dc MG, more general imbalances—where both magnitudes and phase angles deviate—require alternative methods. An effective strategy, can be also adopted in this work, involves assigning opposite resistive values to the positive- and negative-sequence currents, as proposed in [46, 47]. More advanced techniques that additionally account for zero-sequence currents are presented in [45].

The subsequent analysis focuses solely on module a for simplicity, but the methodology can be extended to the other modules similarly. Module a consists of an inductor L and two half-bridges: an ac-side half-bridge (S_{a1}, S_{a2}) and a dc-side half-bridge (S_{a3}, S_{a4}). These two half-bridges are controlled such that only one half-bridge is modulated at any given time, while the other remains clamped, depending on the values of $v_{\grave{a}m}$ and V_{dc}. This results in two distinct operating modes: buck mode and boost mode.

To impose the LFR behavior on each module of the 4-W Y-converter, two sliding control laws are designed, one for each of the buck and boost modes. The objective of each controller is to ensure that the currents $i_{\grave{x}}$ are sinusoidal and in phase with the ac supply

voltages $v_{\grave{x}}$. In each operating mode, $i_{\grave{x}}$ is regulated by controlling the inductor currents i_{Lx}.

6.2.1 Buck mode

When $v_{\grave{a}m}$ exceeds V_{dc}, module a operates in buck mode. In this mode, S_{a3} remains ON, S_{a4} remains OFF, while S_{a1} and S_{a2} switch alternately, as illustrated in Fig. 45a. To impose the LFR behavior, the sliding surface in buck mode, σ_{bu_a}, is defined as:

$$\sigma_{bu_a} = \frac{v_{\grave{a}n}}{r_a} - i_{\grave{a}} \tag{41}$$

Since the circuit is modeled as a POPI system, the following relationship holds:

$$v_{\grave{a}m} i_{\grave{a}} = V_{dc} i_{La} \tag{42}$$

By substituting (42) into (52), the sliding surface σ_{bu_a} can be rewritten as:

$$\sigma_{bu_a} = \frac{(v_{\grave{a}m} - V_{dc})}{r_a} \cdot \frac{v_{\grave{a}m}}{V_{dc}} - i_{La} \tag{43}$$

To ensure the system follows the desired dynamics dictated by $\sigma_{bu_a}(x)$, a hysteresis-based sliding mode control strategy is employed. The control signal u_{bu_a}, which is applied to S_{a1} (with its complement applied to S_{a2}), is designed to maintain the state trajectory within a specified hysteresis band $\pm H_a$. The control law is expressed as:

$$u_{bu_a} = \begin{cases} 0, & \text{if } \sigma_{bu_a} > H_a, \\ 1, & \text{if } \sigma_{bu_a} < -H_a, \\ \text{retain}, & \text{if } -H_a \leq \sigma_{bu_a} \leq H_a. \end{cases} \tag{44}$$

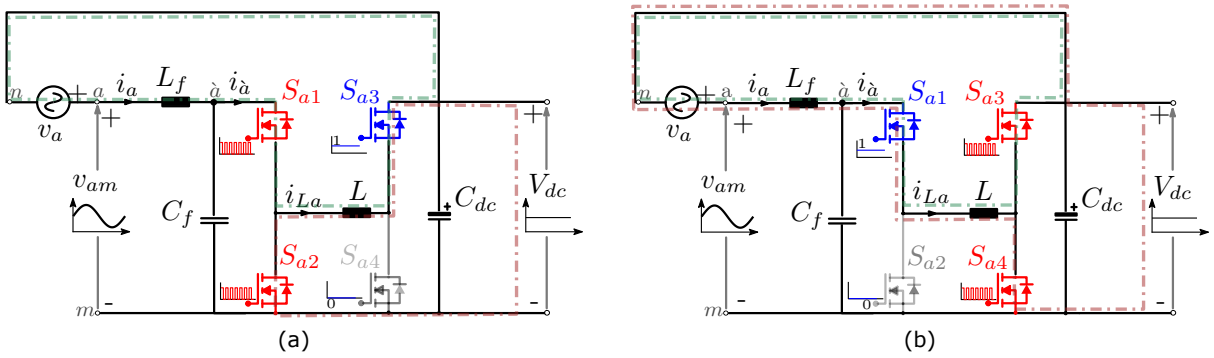


Figure 45: Operation modes of module a of the 4-W Y-converter including current paths: (a) Buck mode ($v_{am} > V_{dc}$); (b) Boost mode ($v_{am} < V_{dc}$).

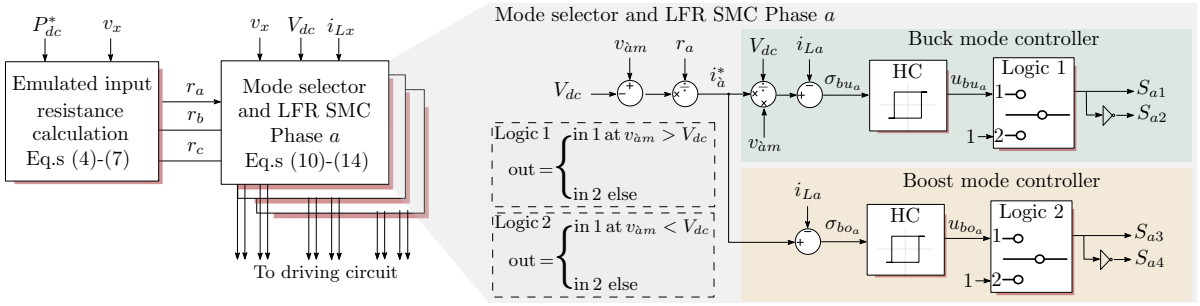


Figure 46: Overall block diagram of the proposed controller, featuring a detailed illustration of the mode selector and the LFR based on SMC for phase a, with key equations highlighted.

6.2.2 Boost mode

Similarly, when $v_{\grave{a}m}$ is lower than V_{dc}, module a operates in boost mode. In this mode, S_{a1} remains ON, S_{a2} remains OFF, while S_{a3} and S_{a4} switch alternately. To impose the LFR behavior, the sliding surface in boost mode, σ_{bo_a}, is defined as:

$$\sigma_{bo_a} = \frac{v_{\grave{a}m} - V_{dc}}{r_a} - i_{La} \tag{45}$$

Consequently, the control signal u_{bo_a}, which is applied to S_{a3} (with its complement applied to S_{a4}), is derived similarly to (44) and is expressed as:

$$u_{bo_a} = \begin{cases} 0, & \text{if } \sigma_{bo_a} > H_a, \\ 1, & \text{if } \sigma_{bo_a} < -H_a, \\ \text{retain}, & \text{if } -H_a \leq \sigma_{bo_a} \leq H_a. \end{cases} \tag{46}$$

The overall block diagram of the proposed controller is illustrated in Fig. 46. The reference power transferred to the dc MG, denoted as P^*_{dc}, is determined by an outer droop controller. Based on this reference, the emulated resistances r_x are defined according to (37) for a balanced grid, and (38), (39), and (40) for unbalanced grid conditions. The calculated r_x values are then processed by the mode selector and LFR based on SMC blocks to generate the control signals u_{bu_x} and u_{bo_x}. For clarity, only the LFR based on SMC of module a is detailed in Fig. 46.

To enhance the performance of the proposed LFR based on SMC and address the limitations of conventional fixed-band hysteresis control, an adaptive time-variant hysteresis band is employed for the following motivations:

- In the hybrid operation of the 4-W Y-converter, smooth transitions between the buck and boost modes are critical to prevent current distortion. A zero hysteresis band at the mode transitions is enforced to eliminate discontinuities and distortions in current waveforms, ensuring seamless operation across both modes.

Table 4: Key parameters of the Four-Wire Y-converter.

Parameter	Symbol	Value
Nominal dc power	P_{dc}	$7\,$kW
dc MG voltage	V_{dc}	$400\,$V
ac grid phase voltage	V_{RMS}	$230\,$V
ac grid frequency	f_o	$50\,$Hz
Switching frequency	f_s	$60\,$kHz
Main inductance	L	$330\,\mu$H
ac filter inductance	L_f	$1200\,\mu$H
ac filter capacitance	C_f	$10\,\mu$F

- Maintaining a nearly constant switching frequency f_s is favorable for practical implementation. A fixed hysteresis band results in variable and potentially high switching frequencies, leading to excessive switching losses and high electromagnetic interference (EMI). The adaptive hysteresis band can maintain a nearly constant f_s, which minimizes switching losses, reduces EMI, mitigates chattering effects, and improves current sampling accuracy.

To achieve these desired control objectives, the adaptive time-variant hysteresis band is defined as:

$$H_x = \begin{cases} \dfrac{v_x V_{dc}}{2 v_{\dot{x}m} L f_s}, & \text{if } v_{\dot{x}m} > V_{dc}, \\ \dfrac{-v_x v_{\dot{x}m}}{2 V_{dc} L f_s}, & \text{if } v_{\dot{x}m} < V_{dc}. \end{cases} \tag{47}$$

6.3 Simulation Results

This section presents the simulation results of the proposed control strategy, validating its performance under diverse operating conditions including balanced and unbalanced ac grid conditions. The converter's specifications and key parameters are summarized in Table 4. The converter is designed to interlink a $400\,$V dc MG with the European LV ac grid and is rated at $7\,$kW, targeting small residential and commercial dc MGs. The hysteresis band is adaptively adjusted according to (47) to maintain a fixed switching frequency of f_s equals $60\,$kHz. This results in a maximum hysteresis band of $\pm 3\,$A, corresponding to a peak-to-peak inductor current ripple of $6\,$A.

6.3.1 Balanced ac grid conditions

The steady-state waveforms of the 4-W Y-converter at nominal power under balanced ac grid conditions are illustrated in Fig. 47. The results confirm that the proposed controller effectively enforces the LFR behavior. The ac grid currents are purely sinusoidal, balanced,

and in phase with the grid voltage, with zero current flowing through the neutral wire. This demonstrates the effective sharing and regulation of the ac grid and inductor currents among the three modules. The time-variant hysteresis band is evident in the inductor current waveforms, ensuring fixed-frequency operation and smooth transitions between buck and boost modes.

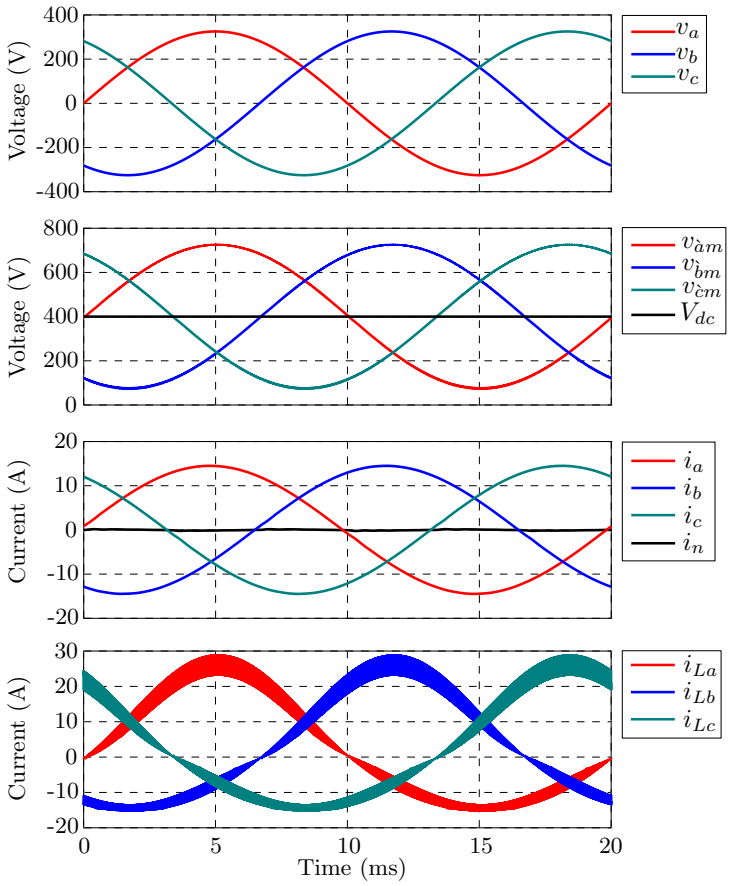


Figure 47: Simulation results of the proposed controller operating at nominal power under balanced ac grid conditions.

The transient behavior of the 4-W Y-converter with the proposed LFR based on SMC under balanced ac grid conditions is illustrated in Fig. 48. Initially, the converter operates at nominal power (7 kW) for two grid periods before the power delivered to the dc MG is reduced to 20% of its nominal value (1.4 kW) for another two grid periods. Finally, the power is stepped back to nominal. The results highlight the fast response and robust performance of the proposed controller for both positive and negative step changes in the reference power. The smooth and rapid adaptation of the emulated module resistances to track the power reference is evident, with all modules maintaining equal resistance values due to the balanced operation. Finally, the ac grid and inductor current waveforms confirm the excellent dynamic response of the proposed controller.

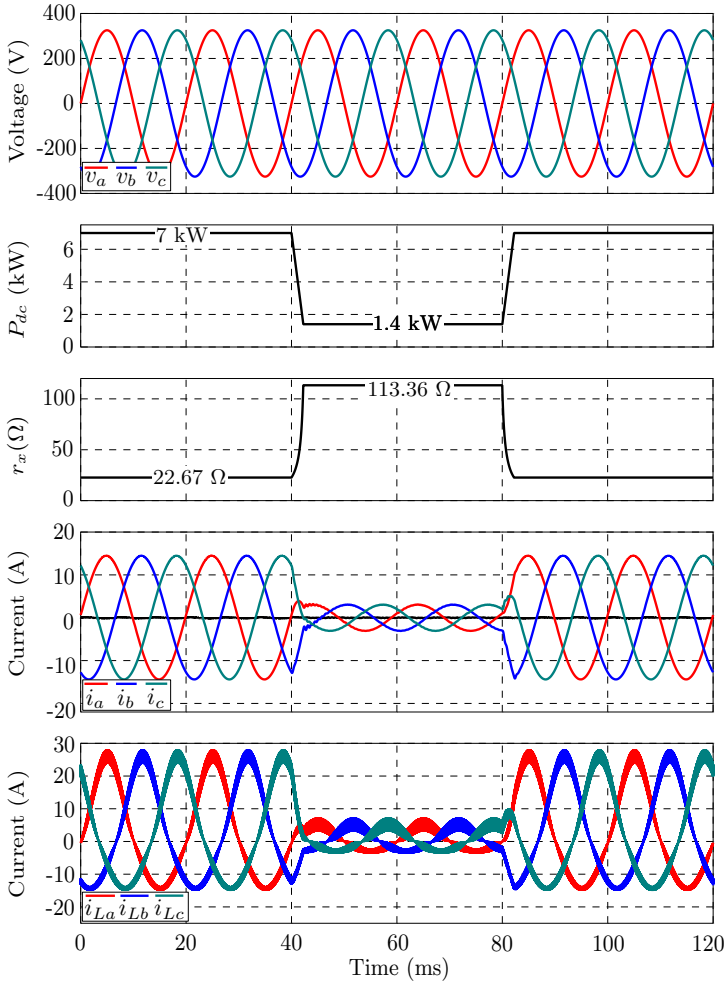


Figure 48: Transient simulation results of the proposed controller under balanced ac grid conditions. The power steps from nominal to 20% after two grid periods and returns to nominal after two more.

6.3.2 Unbalanced ac grid conditions

Fig. 49 presents the steady-state waveforms of the 4-W Y-converter at nominal power under unbalanced ac grid conditions. The results demonstrate that the emulated module resistances can be controlled independently, providing additional flexibility for operating the converter under unbalanced conditions. The RMS phase voltages are set to $V_{\text{RMS}a} = 230\,\text{V}$, $V_{\text{RMS}b} = 210\,\text{V}$, and $V_{\text{RMS}c} = 190\,\text{V}$.

Three control modes are considered under unbalanced ac grid conditions. First, in the constant input current mode, shown in Fig. 49a, the ac grid currents remain balanced despite voltage unbalance. This is achieved by independently adjusting the emulated resistances of each module so that each resistance is proportional to its corresponding grid voltage. Second, in the constant input resistance mode, depicted in Fig. 49b, a fixed emulated resistance value is adopted for all three modules, resulting in grid currents that are proportional to their respective phase voltages. Lastly, in the constant power current

mode, presented in Fig. 49c, equalized power sharing among the modules is achieved by controlling the emulated resistances such that the ac grid current drawn from each phase is inversely proportional to its corresponding grid voltage.

To better highlight the effect of each control mode on the operation of the dc MG, the instantaneous power delivered by each phase, denoted as p_a, p_b, and p_c, along with the resultant instantaneous power delivered to the dc MG, p_{dc}, are presented in Fig. 49. Under both the constant input current and constant input resistance modes, p_{dc} exhibits double-line-frequency power fluctuations around its average value of $7\,\text{kW}$, with the magnitude of these fluctuations being higher in the constant input resistance mode. These power fluctuations induce a corresponding double-line-frequency voltage ripple in the dc MG voltage, which may adversely affect the operation of the droop controllers. Conversely, the constant input power mode ensures ripple-free power flow to the dc MG, making it the preferable choice for interfacing the dc MG with an unbalanced ac grid.

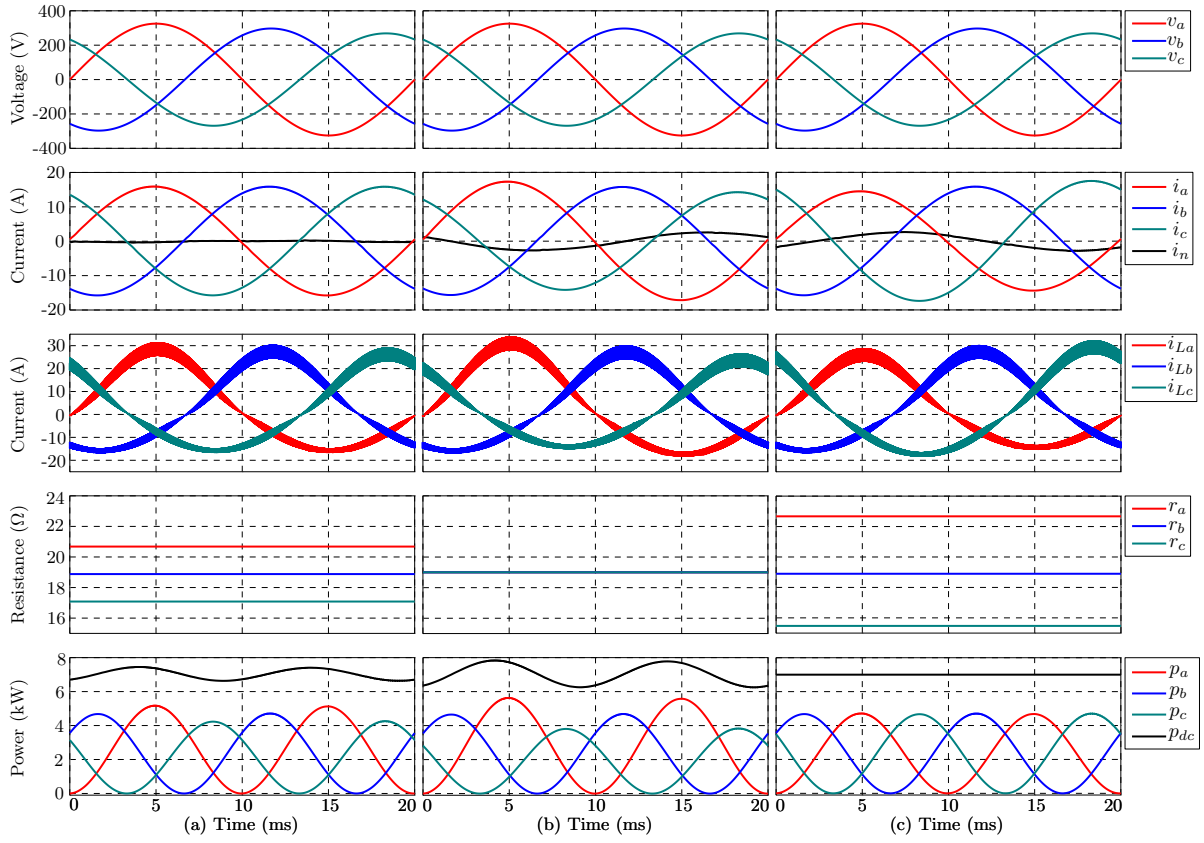


Figure 49: Simulation results of the proposed controller operating at nominal power under unbalanced ac grid conditions: (a) constant input current mode; (b) constant input resistance mode; and (c) constant input power mode. The waveforms illustrate the independent control of the emulated resistances in different modes and highlight the advantage of the constant input power mode in eliminating power fluctuations at the dc MG during unbalanced symmetric ac grid voltages.

6.4 Extension of the proposed Nonlinear Controller to multiport converter scenario

The multiport Y-converter is a three-phase rectifier and is made up of three single-phase modules connected in a star configuration. Each module is an AC-DC six-switch buck-boost converter as shown in the Fig. 50. Each module can be considered as a POPI circuit. Therefore, multiport Y-converter can be modeled by the tetra-port circuit (Fig 51a). SMC can be used to impose a LFR behavior to the multiport Y-converter by emulating each module as a resistance to its respective input phase voltage (Fig 51b). All the power absorbed by these resistances are transmitted to the output port without losses, leading to following power balance equation:

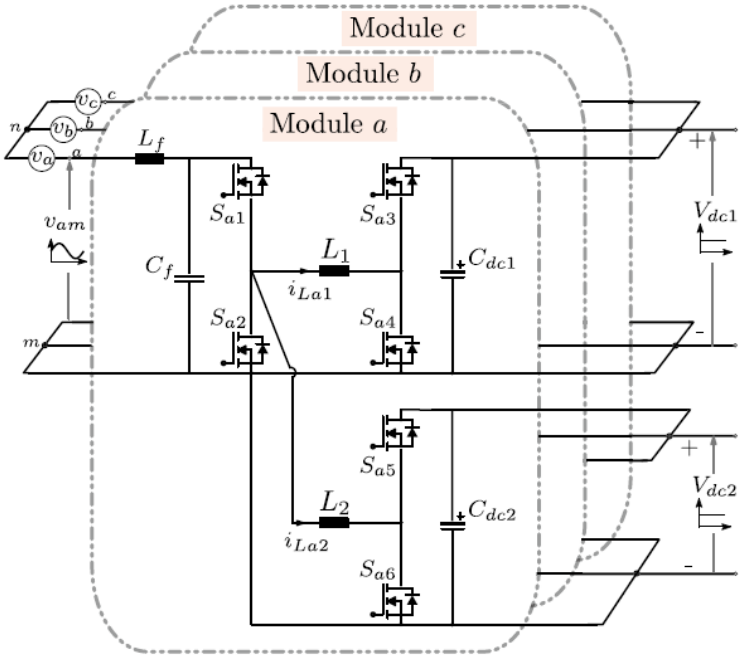


Figure 50: A schematic of multiport Y-converters in a modular form.

$$P_{ac} = P_a + P_b + P_c = P_{dc1} + P_{dc2} \tag{48}$$

For a balanced AC grid, the power delivered by each module is given by:

$$P_a = P_b = P_c = \frac{P_{dc1} + P_{dc2}}{3} \tag{49}$$

Consequently, the emulated input resistance of each module is expressed as:

$$r_{a,b,c} = \frac{3V_{rms}^2}{P_{dc1} + P_{dc2}} = \frac{1}{\frac{1}{r_{(a,b,c)1}} + \frac{1}{r_{(a,b,c)2}}} \tag{50}$$

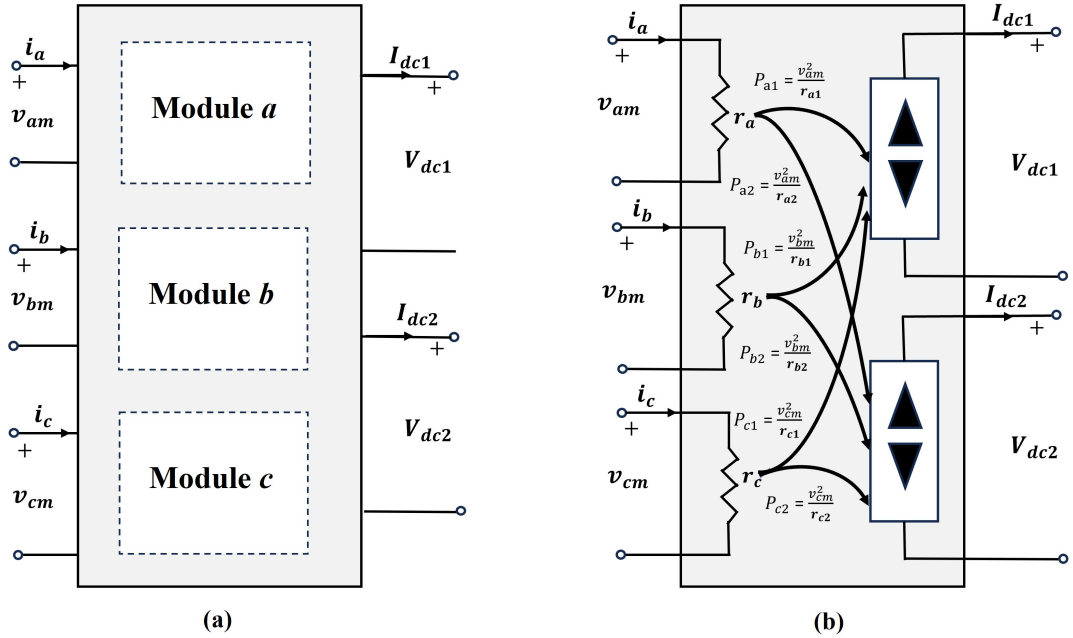


Figure 51: Multiport Y-converter emulated as LFR: a) Tetra-port circuit, b) LFR circuit

where V_{rms} is the rms value of the phase voltage, $r_{(a,b,c)1} = \frac{3V_{rms}^2}{P_{dc1}}$ and $r_{(a,b,c)2} = \frac{3V_{rms}^2}{P_{dc2}}$.

The subsequent analysis focuses solely on module a for simplicity, but the methodology can be extended to the other modules similarly. Module a consists of two inductors L_1 and L_2 along with three half-bridges (Fig. 52): an AC-side half-bridge (Bu_a) and a two DC-side half-bridges (Bo_{a1}, Bo_{a2}). It is assumed that at least one of the DC ports' voltage is lower than the peak of the AC side voltage ($\hat{V}_{am}$), and V_{dc1} is lower than V_{dc2}. Based on these assumptions, the Bu_a and Bo_{a1} half-bridges are under control, ensuring that only one of them is modulated at any given moment, while the other remains clamped based on the values of v_{am} and V_{dc1}, whereas Bo_{a2} will be modulated continuously. This results in two distinct operating modes: buck mode and boost mode.

To impose a LFR behavior to both operation modes, sliding control laws are designed per each mode. The objective of each controller is to ensure that the current i_a to be sinusoidal and in phase with the AC supply voltage v_a. In each operation mode, the current i_a is controlled through the control of current inductors i_{La1} and i_{La2}.

6.4.1 Buck Mode

When v_{am} is greater than V_{dc1}, module a operates in buck mode. In this mode, the Bu_a half-bridge switches, while the Bo_{a1} half-bridge is clamped with S_{a3} ON and S_{a4} OFF, as is depicted in Fig. 53-a. Simultaneously, the Bo_{a2} half-bridge operates with a fixed duty cycle, depending on the ratio between V_{dc1} and V_{dc2}.

Assuming that the switches, inductances and capacitors are considered ideals and ap-

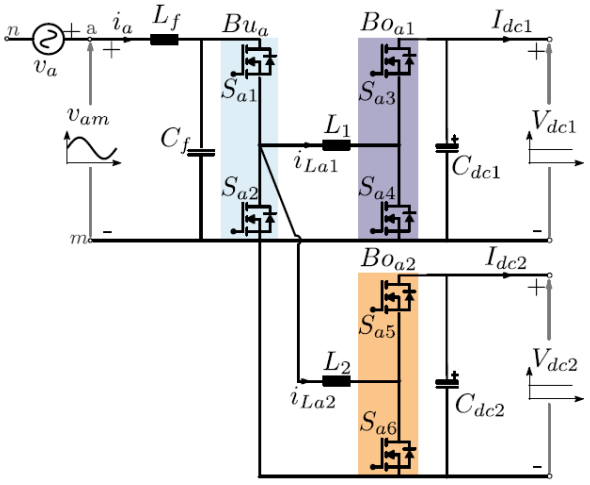


Figure 52: Module a of the multiport Y-converter.

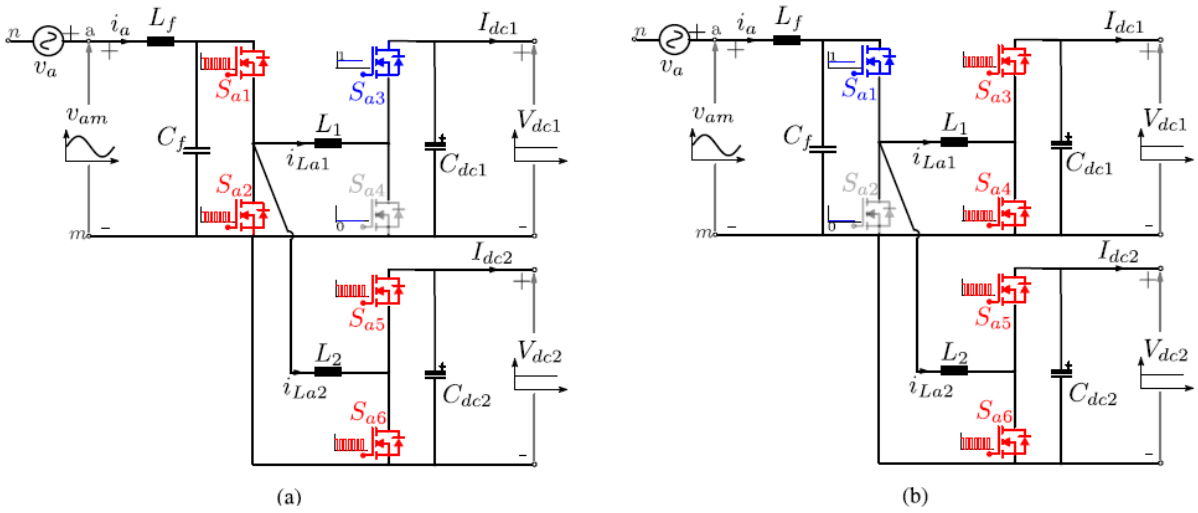


Figure 53: Operation modes of one module of the proposed converter: (a) Buck mode when $v_{am} > V_{dc1}$; (b) Boost mode when $v_{am} < V_{dc1}$.

plying Kirchhoff's Law, module a can be represented by the following switched model:

$$\begin{aligned}
\frac{di_a}{dt} &= \frac{v_{am}}{L_f} - \frac{v_{Cfa}}{L_f} - \frac{r_{Lf}}{L_f} i_a \\
\frac{dv_{Cfa}}{dt} &= \frac{i_a}{C_f} - \frac{i_{La1} + i_{La2}}{C_f} u_{bu_a,buck} \\
\frac{di_{La1}}{dt} &= \frac{v_{Cfa}}{L_1} u_{bu_a,buck} - \frac{V_{dc1}}{L_1} \\
\frac{di_{La2}}{dt} &= \frac{v_{Cfa}}{L_2} u_{bu_a,buck} - \frac{V_{dc2}}{L_2} u_{bo_{a2},buck}
\end{aligned} \tag{51}$$

where $u_{bu_a,buck} = \{0,1\}$ and $u_{bo_{a2},buck} = \{0,1\}$ are the control signals.

In buck mode $i_a = \alpha(i_{L1} + i_{L2})$ ($\alpha = \frac{V_{dc1}}{v_{am}}$ conversion ratio). Therefore, to force the system

behaves like LFR, the sliding surfaces are chosen as follows:

$$\sigma_{bu_a,buck}(x) = \frac{v_{am}}{V_{dc1}} \frac{(v_{am} - V_{off})}{r_a} - (i_{La1} + i_{La2}) \tag{52}$$

$$\sigma_{bo_{a2},buck}(x) = \frac{v_{am}}{V_{dc1}} \frac{(v_{am} - V_{off})}{r_{a2}} - i_{La2} \tag{53}$$

where $x = [i_a, v_{Cfa}, i_{La1}, i_{La2}]^T$ is the vector of state variables.

To ensure the system follows the desired dynamics dictated by $\sigma_{bu_a,buck}(x)$ and $\sigma_{bo_{a2},buck}(x)$, a hysteresis-based sliding mode control strategy is employed. The control signals $u_{bu_a,buck}$ and $u_{bo_{a2},buck}$ are designed to maintain the state trajectory within a specified hysteresis band $\pm H_a$. The control laws are expressed as:

$$u_{bu_a,buck} = \begin{cases} 0, & \text{if } \sigma_{bu_a,buck} > H_a, \\ 1, & \text{if } \sigma_{bu_a,buck} < -H_a, \\ \text{retain}, & \text{if } -H_a \leq \sigma_{bu_a,buck} \leq H_a. \end{cases} \tag{54}$$

$$u_{bu_{a2},buck} = \begin{cases} 0, & \text{if } \sigma_{bo_{a2},buck} > H_a, \\ 1, & \text{if } \sigma_{bo_{a2},buck} < -H_a, \\ \text{retain}, & \text{if } -H_a \leq \sigma_{bo_{a2},buck} \leq H_a. \end{cases} \tag{55}$$

6.4.2 Boost Mode

The Boost mode of operation occurs when v_{am} falls below V_{dc1}. In this mode, the Bo_{a1} half-bridge switches, while the Bu_a half-bridge is clamped with S_{a1} ON and S_{a2} OFF, as depicted in Fig. 53-b. Simultaneously, the Bo_{a2} half-bridge operates with a time-varying duty cycle, depending on the ratio between v_{am} and V_{dc2}. The dynamics of module a can be described by the following switched model

$$\begin{aligned} \frac{di_a}{dt} &= \frac{v_{am}}{L_f} - \frac{v_{Cfa}}{L_f} - \frac{r_{Lf}}{L_f} i_a \\ \frac{dv_{Cfa}}{dt} &= \frac{i_a}{C_f} - \frac{i_{La1} + i_{La2}}{C_f} \\ \frac{di_{La1}}{dt} &= \frac{v_{Cfa}}{L_1} - \frac{V_{dc1}}{L_1} u_{bo_{a1},boost} \\ \frac{di_{La2}}{dt} &= \frac{v_{Cfa}}{L_2} - \frac{V_{dc2}}{L_2} u_{bo_{a2},boost} \end{aligned} \tag{56}$$

where $u_{bo_{a1},boost} = \{0, 1\}$ and $u_{bo_{a2},boost} = \{0, 1\}$ are the control signals. The same procedure as in the case of buck mode will be applied to design the control law.

In the boost mode $i_a = i_{L1} + i_{L2}$. Therefore, the sliding surfaces that forces the system

behaves like LFR are defined as :

$$\sigma_{bo_{a1},boost}(x) = \frac{v_{am} - V_{off}}{r_{a1}} - i_{La1} \tag{57}$$

$$\sigma_{bo_{a2},boost}(x) = \frac{v_{am} - V_{off}}{r_{a2}} - i_{La2} \tag{58}$$

Consequently, the control signal $u_{bo_{a1},boost}$ and $u_{bo_{a2},boost}$, which are applied to Bo_{a1} and Bo_{a2} respectively, are derived similarly to (54)-(55) and are expressed as:

$$u_{bo_{a1},boost} = \begin{cases} 0, & \text{if } \sigma_{bo_{a1},boost} > H_a, \\ 1, & \text{if } \sigma_{bo_{a1},boost} < -H_a, \\ \text{retain}, & \text{if } -H_a \leq \sigma_{bo_{a1},boost} \leq H_a. \end{cases} \tag{59}$$

$$u_{bo_{a2},boost} = \begin{cases} 0, & \text{if } \sigma_{bo_{a2},boost} > H_a, \\ 1, & \text{if } \sigma_{bo_{a2},boost} < -H_a, \\ \text{retain}, & \text{if } -H_a \leq \sigma_{bo_{a2},boost} \leq H_a. \end{cases} \tag{60}$$

The overall block diagram of the proposed controller is illustrated in Fig. 54. The reference power transferred to the DC side, denoted as P^*_{dc1} and P^*_{dc2}, are determined by an outer droop controllers. Based on these reference, the emulated resistances are defined according to (50) for a balanced grid. The calculated resistance values are then processed by the mode selector and LFR based on SMC blocks to generate the control signals $u_{bu_{(a,b,c)}}$, $u_{bo_{(a,b,c)1}}$ and $u_{bo_{(a,b,c)2}}$. For clarity, only the LFR based on SMC of module a is detailed in Fig. 54.

6.5 Simulation Results

This section presents the simulation results of the proposed control strategy, validating its performance under diverse operating conditions including balanced and unbalanced AC grid conditions. The converter's specifications and key parameters are summarized in Table 5. The converter is designed to interface AC grid with DC microgrids (MGs).

The converter´s behavior as LFR under SMC is verified by means of numerical simulations using using MATLAB/Simulink. The proposed controller is depicted in Fig. 54. The parameters of system are outlined in Table 5. Regarding the implementation of SMC, the hysteresis band has been taken $\pm 0.25A$. The performance of the designed controller is validated under diverse operating conditions including balanced and unbalanced AC grid conditions.

The steady-state waveforms of the multiport Y-converter at nominal power under balanced AC grid conditions are illustrated in Fig. 55. The results confirm that the proposed

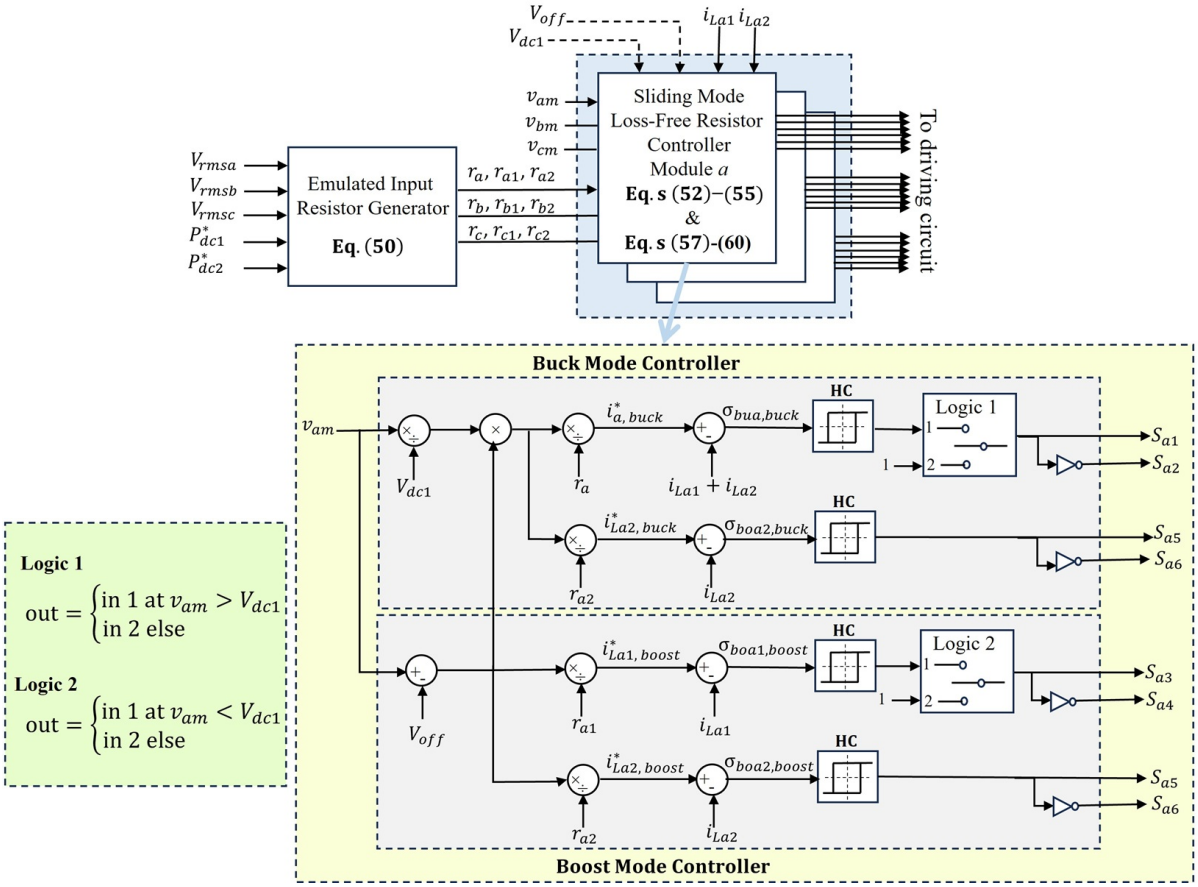


Figure 54: Block diagram of the proposed controller.

Table 5: Key parameters of the Multiport Y-converter used in the simulation results.

Parameter	Symbol	Value
Rated AC power	P^*_{ac}	10 kW
Rated DC power	P^*_{dc1}, P^*_{dc2}	5 kW
AC grid voltage	V_a	230 V
Line frequency	f_n	50 Hz
DC voltage	V_{dc1}, V_{dc2}	360, 400 V
Main inductance	L_1, L_2	500 µH
AC filter inductance	L_f	60 µH
AC filter capacitor	C_f	10 µF

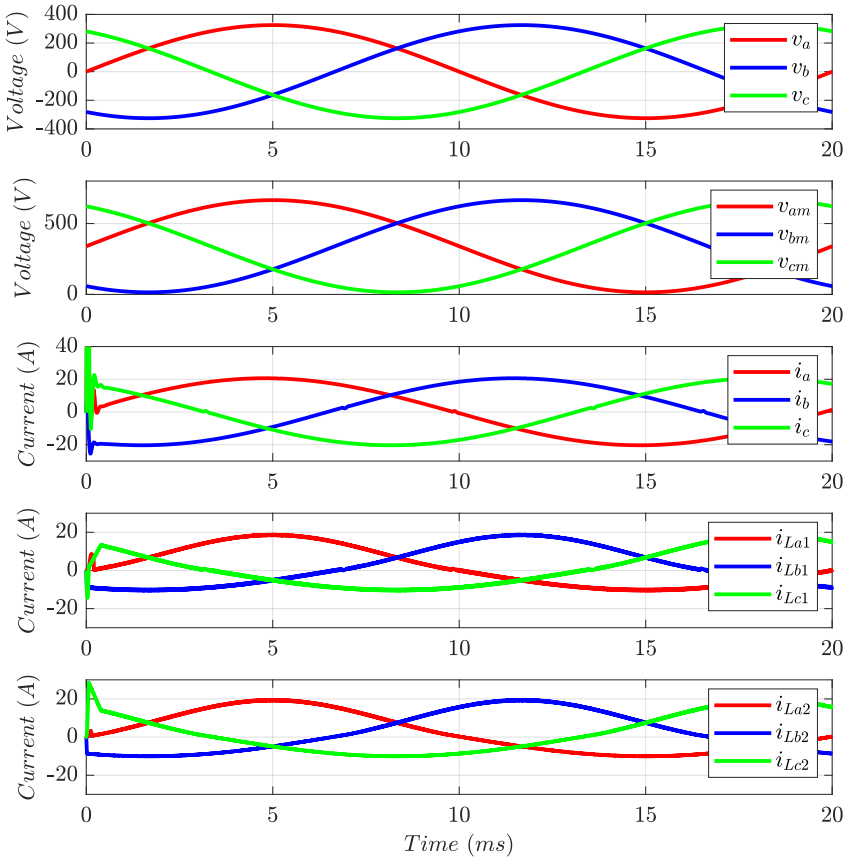


Figure 55: Steady-state simulation results of the proposed controller operating at nominal power under balanced AC grid conditions.

controller effectively enforces the LFR behavior. The AC grid currents are purely sinusoidal, balanced, and in phase with the grid voltage which means that a power factor close to unity is achieved. This demonstrates the effective sharing and regulation of the AC grid and inductor currents among the three modules.

The transient behavior of the multiport Y-converter with the proposed LFR based on SMC under balanced ac grid conditions is illustrated in Fig. 56. Initially, the converter operates at nominal power ($10\,$kW), where both DC MGs are absorbing power from the ac grid, for four grid periods before the delivered power is changed to ($-10\,$kW). This case represents when both DC MGs have a surplus power generation that is fed to the AC grid. In the presented waveforms, the AC grid currents are inverted with respect to their corresponding AC voltages, indicating the power flow direction to the AC grid. Finally, the power is stepped back to nominal value. The results highlight the fast response and robust performance of the proposed controller for both positive and negative step changes in the reference power. The smooth and rapid adaptation of the emulated module resistances to track the power reference is evident, with all modules maintaining equal resistance values

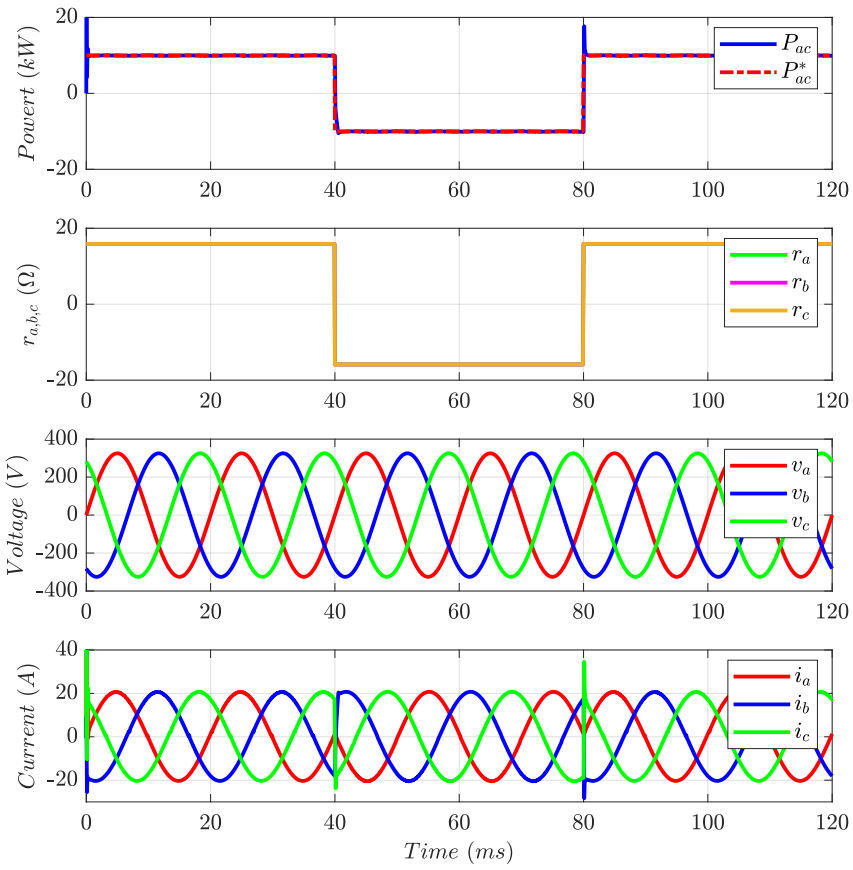


Figure 56: Simulation results of the proposed controller illustrating transient behavior under balanced AC grid conditions.

due to the balanced operation. Finally, the ac grid and inductor current waveforms confirm the excellent dynamic response of the proposed controller.

6.6 Conclusion

This section presents an SMC-based LFR synthesis for unity power factor control of the Four-Wire Y-converter, offering enhanced performance compared to conventional linear controllers in interfacing 400 V dc MGs with ac networks. The proposed control strategy improves dynamic performance with minimal delay, enabling rapid power balancing within the dc MG. Additionally, the controller simplifies the control structure, particularly under unbalanced ac grid conditions. An adaptive time-variant hysteresis band is introduced to ensure smooth transitions between the buck and boost modes of the 4-W Y-converter while maintaining a nearly constant switching frequency. The effectiveness of the proposed controller is evaluated under various operating conditions, including balanced and unbalanced ac grids, as well as transient events.

7 Conclusions

The primary scope of Work Package 3 activities was to investigate and enable MPCs in low-voltage distribution networks, considering both distribution-level and household/residential scenarios. The main outcomes of this work package has been reported in two deliverables: D3.1 [1] and this deliverable D3.2.

This deliverable has presented a comprehensive investigation into low-voltage multiport converters, focusing on rapid prototyping, experimental validation, performance evaluation under realistic mission profiles, and advanced control design. First, a flexible rapid-prototyping setup was developed, incorporating two types of half-bridge modules: commercial Imperix PEB8024 modules (with C2M0080120D SiC MOSFETs) for the boost stages, and fully custom half-bridge modules (with UF4SC120023K4S SiC MOSFETs) for the buck stages. The custom modules' lower on-state resistance and adjustable dc□link capacitance enabled precise tuning of conduction losses and reactive power requirements, while the Imperix modules provided rapid development capability for the boost circuits.

Next, both the symmetric and asymmetric variants of the multiport Y-converter were experimentally validated under steady-state and dynamic conditions. The testbench features bidirectional ac and dc programmable power supplies, real-time control platforms, and high-precision measurement instruments—closely emulated real-world operating scenarios. Experimental waveforms confirmed that both converters maintained balanced three-phase grid currents with low THD during fast transients and various load distributions. In the symmetric configuration, uniform power sharing and consistent port behavior were observed, whereas the asymmetric configuration demonstrated efficient management of differential power flows by leveraging its hardware asymmetry and flexible control laws. Efficiency curves derived from calibrated power meter measurements revealed high conversion efficiency across a wide power range for both topologies.

To quantify the advantages of MPCs in a renewable energy context, a mission-profile-based performance evaluation was conducted for interconnecting 400 V dc microgrids with the European low-voltage ac grid. Two design approaches were compared: separate two-port Y-converters versus a single integrated multiport Y-converter. A multi objective Pareto optimization framework explored trade-offs between average efficiency and power density, taking detailed loss and volume models into account. Results showed that the MPC topology achieves superior average efficiency during dc-to-dc power transfer by eliminating the intermediate ac-stage losses inherent in the 2Y configuration. Both designs reached high efficiency and power density levels, but the MPC consistently outperformed the 2Y approach under realistic mission profiles, confirming its potential as a compact, cost effective interface for future dc microgrid deployments.

Finally, a novel loss-free resistor hysteresis controller was proposed for the Y-converter to overcome the dynamic response limitations of conventional linear controllers. By generating switching actions directly from instantaneous system measurements, the hysteresis-based scheme delivers faster transient response, robust stability across varying operating points, and simple implementation without complex compensation networks. The controller was verified in simulation first on a two-port converter and then extended to the multiport scenario, demonstrating precise current and voltage regulation, rapid response to load changes, and reliable operation under both balanced and unbalanced grid conditions.

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