iPLUG

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Comparison and experimental validation of MV multiport converter

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List of Acronyms

AC	Alternating current
CHB	Cascaded H(full)-bridge
CHIL	Control Hardware in the loop
DAB	Dual-active bridge
DC	Direct current
DN	Distribution network
EMI	Electromagnetic Interference
ESOP	Enhanced soft-open point
ESS	Energy storage system
FB	Full(H) bridge
FRT	Fault ride through
GaN	Gallium Nitride
HfB	Half bridge
HFT	High-Frequency Transformer
iM2DC	Isolated multilevel modular dc converter
IMPC	Isolated Multi-Port Converter
ISOP	isolated soft-open-point
L/HF	Low/High frequency
L/MV	Low/Meduim voltage)
MAB	Multi-acitve bridge
MD-RCC	Multi-Dimensional Ripple Correlation Control
ML	Multilevel
MMC	Modular multilevel converter
MPC	Multiport converter
MPSM	Multi-Phase Shift Modulation
MPSM	Multi-Phase Shift Modulation
NLM	Nearest Level Modulation
QAB	Quadruple Active Bridge
PI	Proportional integral
PSC	Phase Shifted Carrier
PSM	Phase Shift Modulation
PWM	Pulse width modulation
RCC	Ripple Correlation Control
SiC	Silicon Carbide
SM	Sub module
SOP	Soft open point

STATCOM	Static synchronous compensator
SVPWM	Space Vector Pulse width modulation
TAB	Triple-active bridge
VSC	Voltage source converter
ZVS	Zero Voltage Switching

List of Nomenclatures

C_{DC}	DC capacitor
C_{eq}	Equivalent capacitor
C_{SM}	Submodule capacitor
C_x	Number of components in configuration x
F_s	Switching frequency
f_{Sw}	Switching frequency
i_{DC}	DC current
i_l^j	Lower arm current
i_{pr}	Prioritized current
i_{qd}	Grid current
i_u^j	Upper arm current
L	Inductance
L_f	Filter inductor
m	MMC AC/DC voltage modulation ratio
M_x	Number of DC/DC modules in configuration x
N_{arm}	Submodules per arm
N_x	Number of AC/DC SMs in configuration x
P	Active power
Q	Reactive power
R	Resistance
S	Converter power
t	Time
T.C.	Transformer cores
T.W.	Transformer windings
V	PCC voltage
V_{Cl}^j	Applied lower arm voltage
V_{conv}	Converter voltage
V_{Cu}^j	Applied upper arm voltage
V_{dc}	DC port voltage
V_l^j	Lower arm voltage
V_{SM}	SM capacitor voltage
V_{sum}	Additive voltage
V_u^j	Upper arm voltage
W	Energy
X	Reactance
α_i	Weighting parameter

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1 Executive summary

This report, Deliverable 2.2 of the iPLUG project, overviews the work that has been carried out in WP2 on comparison and experimental validation of medium-voltage multiport power converters (MPCs). For this, various candidate topologies with distinctions in configuration, isolation and converter cells to build the MV topology are compared in order to select the best alternative for MV application. From the comparison, a partly-isolated topology, which combines the good characteristics of the fully non-isolated as well as the fully isolated topologies in terms of performance in normal and fault conditions, flexibility for varying voltage and power levels, and number of components, is selected. Finally, a small-scale and slightly modified laboratory prototype is developed for the selected topology and its performance in both normal and fault conditions is tested to verify the successful operation of the topology.

2 Introduction

In line with the EU's commitment to global climate action under the Paris Agreement, modern power systems are increasingly dominated by clean energy sources with net-zero greenhouse gas emissions to achieve the aim of being climate-neutral by 2050. Hence, there is an unquestionable trend to increase the penetration of renewables to unprecedented levels both at transmission and distribution level. In this regard, European Union is targeting a 40% share of renewables by 2030 with the intention to achieve much higher targets by 2050. With this effort in the transition towards more renewable energy production, the use of power converters to interface these sources to the grid is correspondingly increasing. The type and level of these renewable sources is especially high at distribution level and hence the demand for power electronics based solutions to increase the capacity and reliability of the grid is even more important.

At distribution level with significant penetration of renewable sources (such as solar PV and wind power plants), several industrial loads, electrical vehicle charging stations, and energy storage units, power electronics play a vital role in enhancing integration of renewables and energy storage systems, optimal use of the distribution network, and connection of various loads at different voltage levels both with AC and DC. Some of the power-electronic solutions discussed in the literature in the distribution grid for capacity enhancement, improved flexibility, and better controllability include the use of Soft-Open Point (SOP), smart transformers and multiport converters [1–3]. When isolation is required in some of these configurations for medium or high voltage applications and when varying voltage levels are involved, high-frequency based DC-DC converters are important building blocks of the converters. In this regard, dual-active bridge (DAB) based DC-DC converter is the most common configuration. On the other hand, the use of DC-DC converters with multiple active-bridges has the advantage of reliability during faults and reduce the number of modules for medium or high power application [4, 5]. In line with this, WP2 aims to develop suitable multiport converter topologies and their control schemes to enhance MV distribution system's efficiency and utilization. Different multiport converter structures will be investigated and ranked, based on the specific functionalities to be provided to the distribution grid. To achieve this objective, comparison and evaluation of multiport power converters has been performed to select a topology suitable for medium voltage application. Specifically, this report documents tasks 2.3 and 2.4 of WP2 and a summary of the work include:

1. Evaluate and rank multiport converter topologies for MV application
    - review of various multiport candidate topologies for MV application
    - comparison and selection of the best topology based on design flexibility, number

of needed components, fault handling and dynamic performance.

- optimization demonstration of isolation stage with triple-active bridge converter as an example.

2. Laboratory validation of selected topology

- Dynamic performance test validation of a non-isolated MV-MPC based on full-bridge(FB) MMC by Typhoon HIL's control- hardware in the loop (CHIL) setup confirming the practical feasibility of the topology.
- Dynamic performance test validation of the selected partly-isolated MV-MPC based on FB-MMC similar to the previous point but with the addition of an isolated DC-port and a modified control strategy. Here, the prototype is developed using all hardware as it will be detailed in Chapter 6.

3 Identification of a topology for medium-voltage laboratory verification

3.1 Application Specifications

Work Package 2 focuses on the development of multiport power converter solutions for medium voltage applications. Valuable MPC applications are detailed in D1.1. One medium voltage application outlined in D1.1, which will be the focus of this deliverable, is the Enhanced Soft Open Point (ESOP). Figure 1 exhibits an overview of the MPC configuration within an ESOP application.

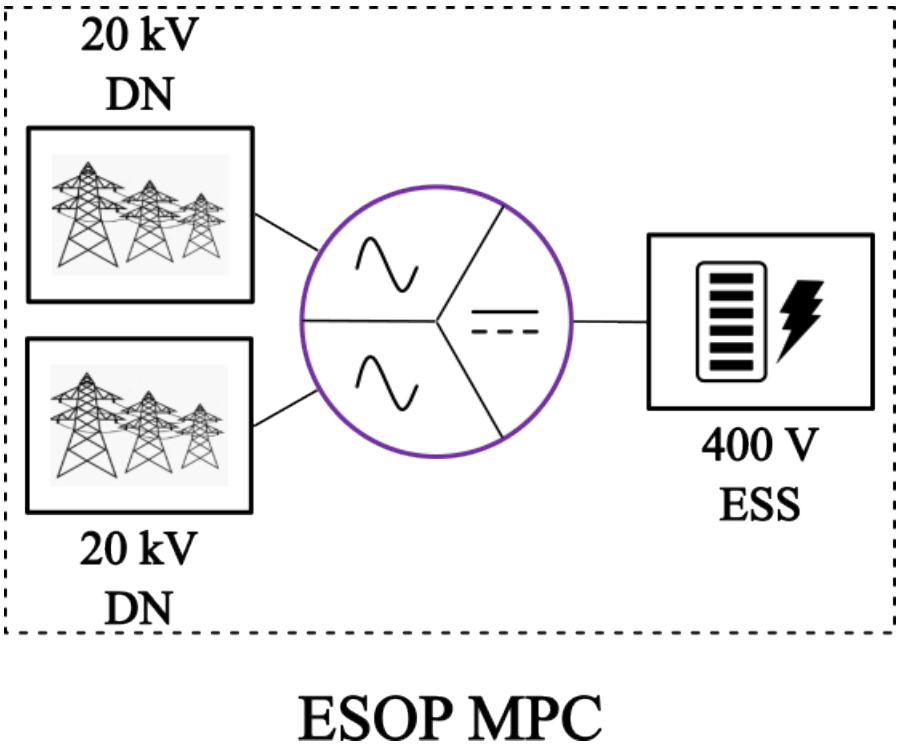


Figure 1: Enhanced soft open point application diagram.

The MV ESOP application involves the interconnection of two MV AC distribution network (DN) feeders with a low voltage (LV) DC energy storage system (ESS). The objective of the MPC ESOP is to interconnect the DN feeders with the DC port to optimize the power flow between the three ports to increase low carbon energy utilization, minimize network costs, and maximize energy availability. Low carbon energy utilization is increased by minimizing steady-state voltage variations of the DN feeders that may constrain distributed energy resources. The supply of customers with cheap local low carbon energy and minimization of network reinforcement can support low network costs. Energy availability can be supported by the collocated ESS, particularly if the MPC is capable of islanded operation. All of this functionality should be achieved with the parallel objective of fault current containment.

Two MV ESOP cases have been specified to represent different voltage gain cases. Case 1 represents a high voltage gain case where there is a large difference in the voltage of the AC DN feeder port with respect to the DC port. Case 2 represents a lower voltage gain scenario. The voltage and power specifications of each port (detailed in Table 1) are derived from a specific DN's characteristics and corresponding ESS sizing, both provided by Spanish DSO Anell. The power level is low due to the derivation from a transformer specification but serves as a conservative low sizing, which highlights the increasing suitability of the MPC topologies as the power level increases.

Table 1: Port specification for the two Enhanced Soft Open Point Cases.

Port		Voltage		Power	Bidirectional
		Case 1	Case 2		
1,2	AC DN Feeder	20 kV	5 kV	400 kVA	Yes
3	DC ESS	400 V	800 V	100 kW	Yes

To fulfill the application specifications, the topology will need to:

- Interconnect widely different voltage levels. To achieve this, the AC ports will need to be scalable to integrate the medium voltage level, a large voltage gain will be required to step the MV down to LV, and isolation is expected to be required to contain the potentially high fault current levels.
- Achieve bidirectional and decoupled power capability across all three ports. This will support the optimized transfer of energy across the feeders for steady-state and dynamic objectives.
- Ensure reliability and fault-tolerance that have a low-likelihood of failure and are capable of continuing operation in the case of loss of components, submodules, or ports.

All of this functionality should be achieved with minimal cost, size, and operational complexity and at maximum efficiency.

3.2 Exploration of Feasible Conversion Approaches

iPlug Deliverable 1.1 [6] introduced the range of MPC solutions that may be suitable for MV power system applications. The previous work highlighted that conventional two-port non-isolated AC/DC converters were suitable to be scaled to MV levels but that the extension of these configurations to multiport non-integrated solutions would be associated with large numbers of components. Isolated converters were found to offer desirable fault tolerance [7], the limitation of harmonic transfer between medium and low voltages [1], and high voltage gain capability but at the cost of increased port coupling and operational complexity.

They were deemed to require high numbers of components for simple applications but they may be suitable for higher voltage gain applications. Partially-isolated converters were less widely explored for MV levels but may offer a mixture of the benefits of non- and fully-isolated topologies.

The feasibility of a range of topologies for the specific cases detailed in Section 3.1 will be explored in the following subsections. The most suitable topology from the partially-isolated family and the most suitable from the isolated family will be identified from the review, both of which will be carried forward for a detailed analysis in Section 3.3.

Some single-stage converter approaches exist that are capable of interfacing multiple ports in a single conversion device (e.g. direct isolated matrix converters) but they don't offer easy integration of additional ports and experience coupling between ports that could limit the operational capability of the MPC [8]. To ensure the desired decoupling of the MV DN feeders from the LV ESS port, only multi-stage topologies will be considered here-on (which are associated with increased capacitance, sensing, and processing requirements compared to single-stage solutions [9]).

3.2.1 Partially-isolated Topologies

The MV AC ports will require a multi-level (ML) conversion configuration to enable the use of cost effective LV rated switches. ML AC/DC converters are often associated with a modular design, flexible operation, and high quality power output [10]. While Cascaded H-bridge (CHB) configurations offer simple and low component multi-level topologies, they cannot support an intermediate DC bus, which is deemed to be necessary to integrate the DC port of the partially-isolated topology. As a result, modular multi-level converter (MMC) configurations will be pursued, which are widely implemented in back-to-back configurations to integrate two AC ports to one another.

MMC submodules (SMs) can be configured as either half- (HfB) or full-bridge (FB). HfBs are composed of only two switches per SM, which enables the modulation of 0 or positive voltages. This results in an intermediate voltage bus that must operated at a fixed voltage, two times larger than the peak AC port voltage. In contrast, FBs are composed of four switches per SM, which enables the modulation of 0, positive, or negative voltages. The ability to modulate negative SM voltages enables the MMC to operate in AC voltage boost mode, where the intermediate DC voltage is lower than the AC port voltage. For fixed AC port voltages, this offers the ability to operate with a lower intermediate voltage and the potential to decrease the number of SMs required in the DC stage. Several papers have explored the optimization of an active front end converter (some also considering a DC/DC stage to integrate one MV AC DN port with a LV DC port) [11–13]. The key conclusions from these studies include:

- HfB MMCs need to be adapted for different AC port voltages using a transformer, whereas, FB MMCs have a flexible modular design that can be adapted for different port specifications [11].
- FB efficiency is degraded for very high modulation indices ($V_{DC} << V_{AC}$) due to large arm currents. A mid-modulation index can offer a balance of efficiency vs low component number [11].
- Hfb SMs have better reliability than FB SMs due to the lower number of components, however, FB MMCs benefit from the robustness to survive SM failure and therefore have a lower mean time between failure compared to HfB MMCs [11].
- FB MMCs are also fault tolerant due to their three voltage level modulation ability, which mitigates the requirements for LV fuse and circuit breakers that would otherwise be necessary [11].
- The SM capacitor requirement increases as the intermediate DC voltage level reduces, which has a large impact on MMC size and weight [12].
- Voltage ripple and harmonics also need to be considered when choosing a modulation index [13].

An isolated conversion stage is expected to be required to provide the large voltage gain and fault current protection properties needed to integrate the LV DC port to the MV intermediate DC bus. An example of an isolated DC/DC converter is a dual-active bridge (DAB) converter, which is pictured in Figure 2. A DAB is an isolated, bidirectional, and highly efficient two port DC/DC converter [14] whose power flow can be easily controlled by phase shift.

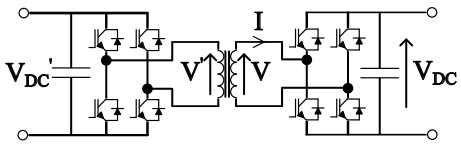


Figure 2: Dual-active bridge topology.

Although the FB MMCs can operate with a low intermediate DC voltage, the modulation ratio should be limited to avoid the degradation of the converter efficiency and capacitor sizing, meaning that a standard DAB module (using cost-effective LV rated switches) will not be able to link the two DC voltages [15]. Instead, series-connection of the DAB modules can be considered.

The isolated Modular Multilevel DC Converter (iM2DC) (pictured in Figure 3) offers series connection of half-bridge or full-bridge submodules to convert a medium voltage DC voltage to a high-frequency (HF) AC voltage. The AC voltage is then fed to a transformer winding

whose secondary side is interfaced by a similar (but not necessarily identical) HF AC to DC voltage conversion stage [16].

Using FB SMs, the iM2DC is also capable of modulating three voltage levels, which supports the rapid dissipation of cable inductor energy and the independence of AC and DC voltages [16]. However, this topology incorporates a large number of components (including six sets of series SMs and three two-winding transformers) and requires a degree of symmetry around the isolation stage which does not match the medium voltage-low current to low voltage-medium current characteristics of the MPC.

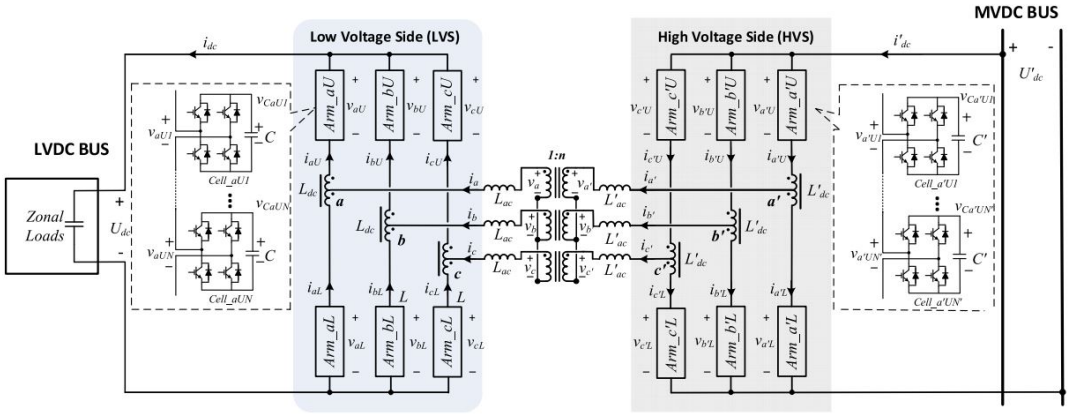


Figure 3: Isolated modular multilevel DC converter topology. Figure from [7].

Alternatively, an Input-series Output-parallel (ISOP) multi-DAB configuration [7] could be used, which better matches the MPC ESOP's voltage and current characteristics. An example of an ISOP configuration is pictured in Figure 4. The ISOP connects DAB modules in series on the higher voltage side, utilizes the fundamental properties and control of the DAB module to transfer power from one side to another, and connects the lower voltage side in parallel. The ISOP configuration allows the use of identical LV-rated HF switches on both sides of the converter (assuming that the low voltage fits within the rating of the switch). ISOP has been shown to exhibit soft switch on (with an inductor on the primary side), which can offer lower switching losses, higher switching and transformer frequencies, and therefore the lower sizing of passive components [17]. The higher switching frequency also mitigates harmonic current and voltage components, allowing the smaller sizing of DAB module capacitors.

A MV AC to LV DC application using MMC plus ISOP configuration was found to achieve a reduced number of switches and HF transformers compared to a Solid-state Transformer in [18]. The number of components for this application was found to reduce further by using a FB MMC with low intermediate DC bus in [11].

Both of the two feasible DC/DC conversion approaches for the intermediate bus to LV port offer good scalability to integrate large and variable voltage levels (depending on the

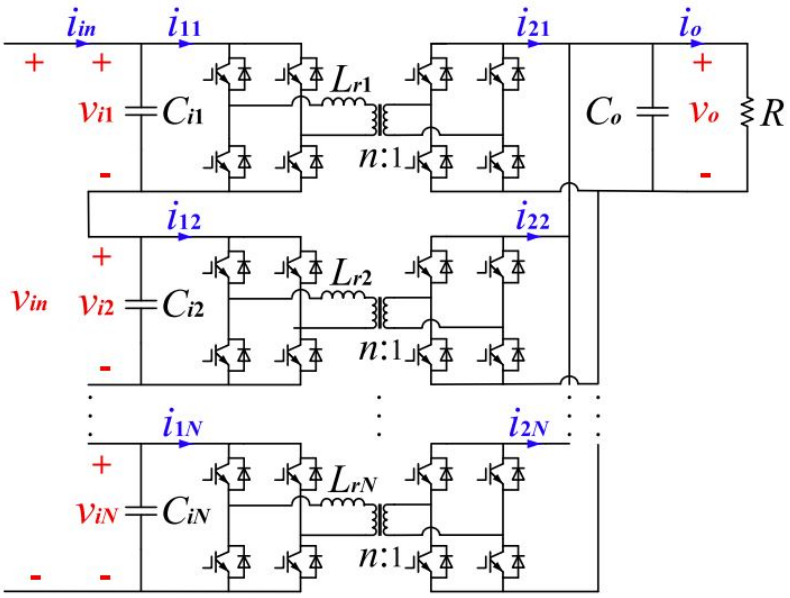


Figure 4: Input-series Output-parallel converter topology. Figure from [19]

specific application). However, they differ in terms of the following key features.

The iM2DC:

- Is expected to require a large number of components and have less suitable voltage and current characteristics for the given DC/DC conversion.
- A higher device rating is required to enable devices to support the sum of AC and DC components, which degrades the efficiency, constrains switching and transformer frequencies, and increases the requirement for passive component sizing [17].
- Negative voltage modulation allows the decoupling of DC and AC sides. Although a MV fault will isolate the LV port, a LV fault will simply be observed as a load change allowing the MV port to maintain normal operation [7].

While the ISOP:

- Is capable of relatively simple decoupled operation of DAB modules, which fit the voltage and current characteristics of the given DC/DC conversion well.
- Requires fault identification to switch to fault mode (which drives the shutdown of the entire two-port ISOP converter) in the case of both LV and MV faults [7].
- The series connection of DAB modules on the medium voltage side may degrade converter robustness to switch failure.

Although the ISOP converter exhibits worse two port fault characteristics, fault behavior hasn't been explored for MPC configurations, where it may be possible to shutdown

the ISOP converter but maintain back-to-back operation of the two MMCs (and therefore achieve similar fault characteristics as the iM2DC). Considering this feature, the simplicity of operation, and the suitability of the configuration for the MV DC to LV DC application, the ISOP will be selected as the DC/DC stage of the partially isolated converter. Figure 5 exhibits the configuration of this winning topology from the partially-isolated family, which will be carried forward for a detailed comparison with the winner from the isolated family.

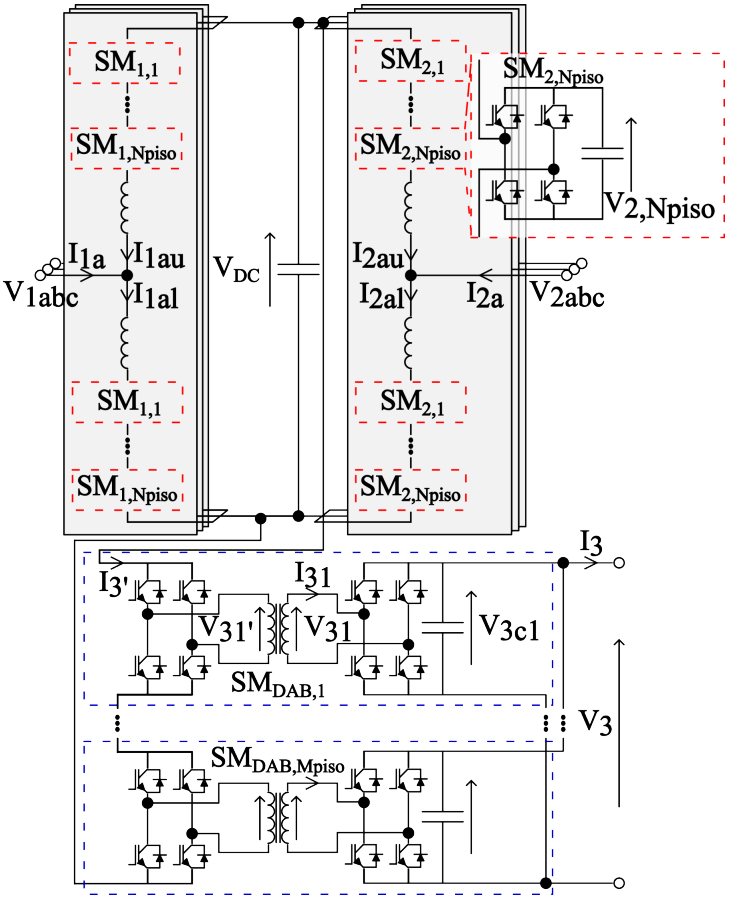


Figure 5: Partially-isolated topology winner: Back-to-back full-bridge modular multilevel converter with input-series output-parallel dual-active bridge topology.

3.2.2 Isolated Topologies

To achieve isolation of all ports from one another, triple- (TAB) or multi-active bridge (MAB) modules will be required to interface the three ESOP ports together. A TAB (pictured in Figure 6) uses the same operating principles as a DAB; a DC input voltage is converted to a HF AC voltage using an active bridge module. Three active bridge modules are interconnected using three independent windings around a single transformer core. A MAB extends the configuration by adding additional active bridge and winding pairs to integrate every additional port.

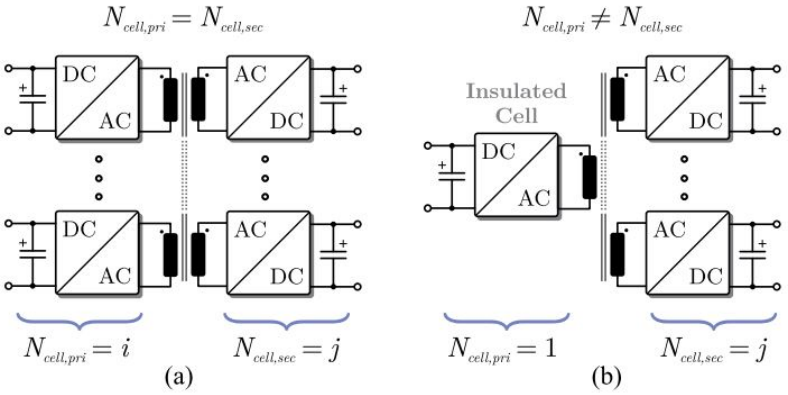


Figure 6: Triple/multi-active bridge module. Figure from [14]

TABs and MABs possess similar characteristics to DABs: isolation by the HF transformer, voltage gain via turns ratio, bidirectional power flow via phase shift control, and zero voltage switching ability. However, the topologies experience more complicated magnetic coupling and circulating current issues that worsen with increasing numbers of ports [20]. Control solutions exist to mitigate these issues but can depend on internal models that have varying degrees of accuracy and complexity.

Extending the iM2DC configuration to accommodate three DC ports (each port using three HF AC phases that would each be converted using an allocated MMC leg) would require a large number of components (at least 50 % more compared to a DAB configuration) and complex operation just to establish DC voltages. Additional stages would be required to convert the DC voltages to the MV AC ports. Such a configuration will not be considered further.

Alternatively, multiple TAB or MAB modules can be configured to integrate multiple ports with varying voltage and current characteristics. Two configurations of a multi-MAB configuration derived from [21] are pictured in Figures 7 and 8. Both configurations use a CHB ML AC/DC conversion approach due to the independence from a single intermediate DC bus and instead the direct connection of active bridges to the AC/DC SM's voltages. The CHB offers half the number of cells compared to a FB MMC, simple operation, and smaller SM capacitance [22, 23].

Figure 7 uses a seven port MAB module to interface a group of three CHB SMs from one AC port to an identical group of three CHB SMs from the other AC port. An additional winding and active bridge pair is allocated in the MAB module to feed the DC port. Additional modules are then connected to interface the additional groups of CHB SMs that make up the MV AC port (as well as contributing to the DC port). The MAB configuration is flexible to be fit to the voltage and current characteristics of the application, where more CHB SM-linked AB pairs can be grouped with a single DC port-linked AB as the ratio of AC port power

to DC port power increases. Figure 8 introduces an additional intermediate DC bus that interfaces asymmetrical CHB SM-linked MAB modules and feeds the DC port (either directly or through its own DC/DC converter). Both configurations can maintain power transfer in the case of CHB SM or active bridge failures (but at the cost of SM capacitor imbalance).

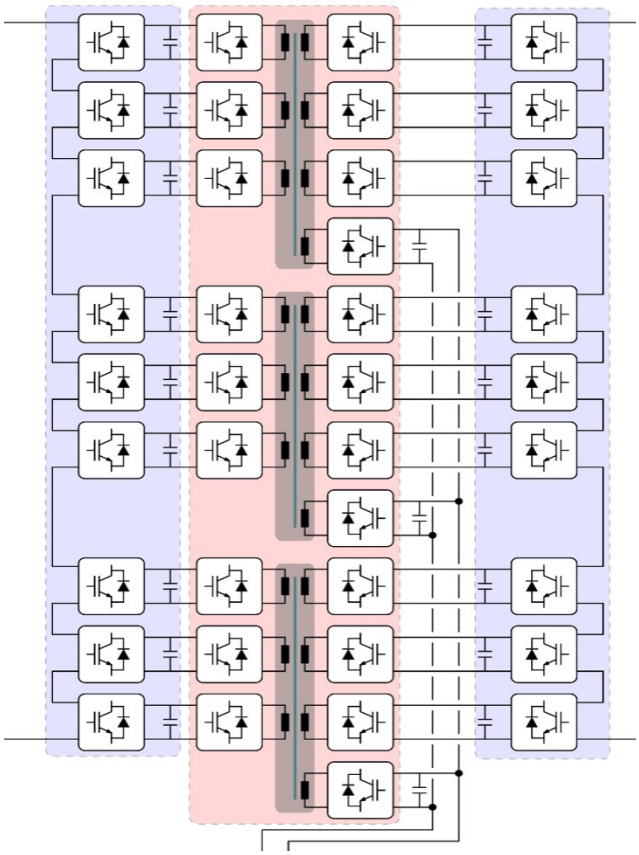


Figure 7: Multi multi-active bridge topology with intermediate AC stage. Topology derived from [21]

The topology in Figure 7 is selected as the winner of the isolated family due to the lower number of components compared to that in Figure 8 while maintaining similar reliable operational characteristics.

3.3 Comparison of Winning Topologies

The previous sections have refined reviewed topologies to identify the most feasible partially-isolated and isolated solutions to fulfill the ESOP MPC application. In this section, a detailed comparison of the topologies pictured in Figure 5 and Figure 9 is presented for the purposes of selecting a final topology for laboratory verification. The detailed comparison in the following subsections includes an analysis of component numbers for the two ESOP cases and a qualitative discussion and scoring of the critical operational characteristics.

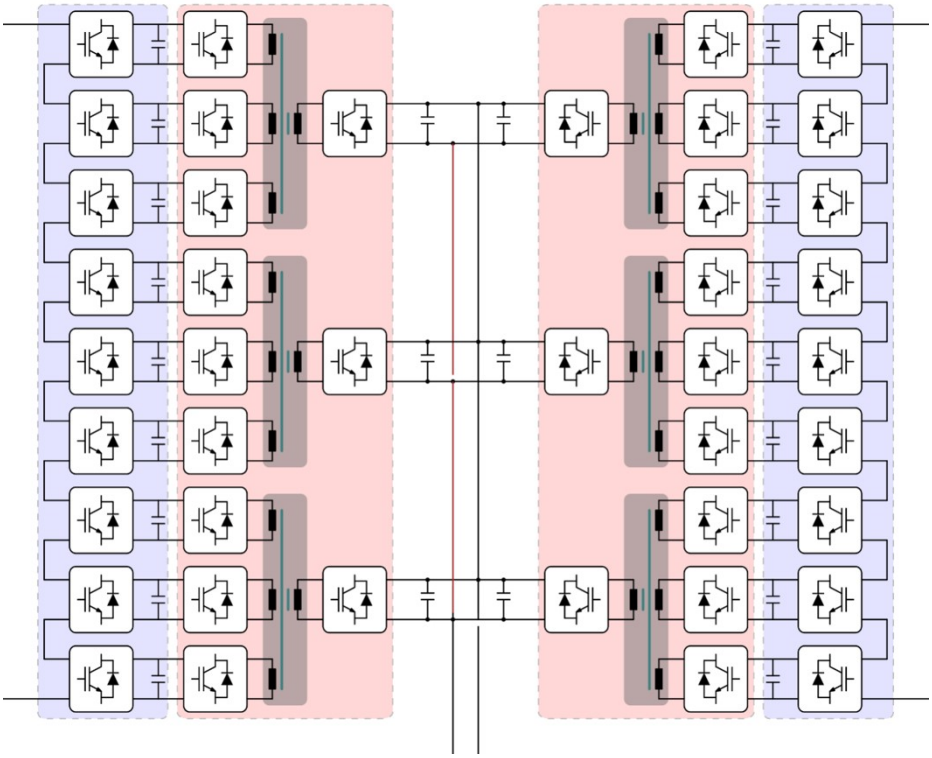


Figure 8: Multi multi-active bridge topology with intermediate DC stage. Topology derived from [21]

3.3.1 Number of Components

The number of components of each topology is compared as a function of different variable parameters as a proxy for the size and cost. The topologies are examined for both ESOP cases: Case 1 requires the larger voltage gain from 20 kV AC to 400 V DC, while Case 2 requires a lower voltage gain from 5 kV AC to 800 V DC.

The voltage blocking ability of low frequency FB switches is assumed to be 3.3 kV and the voltage blocking ability of high frequency active bridge switches is assumed to be 1.2 kV. Both switch types are limited to operate with a utilization factor of 0.65. These specifications represent an optimal setting utilized for a two port MV AC to LV DC MMC plus ISOP configuration in [11]. Table 2 details the exact voltage and current requirements of the topology components considering these voltage blocking abilities and the sizing of the topologies for Case 1.

Derivation of the Partially-isolated Topology's Components Not considering the DC voltage level, the number of MMC FB SMs required to interface to one phase of the MV AC voltage is defined by $N_{P.Iso,AC}$

$$N_{P.Iso,AC} = 2 * ceil(\frac{\hat{V}_{AC}}{V_{SM,FB}}) \quad (1)$$

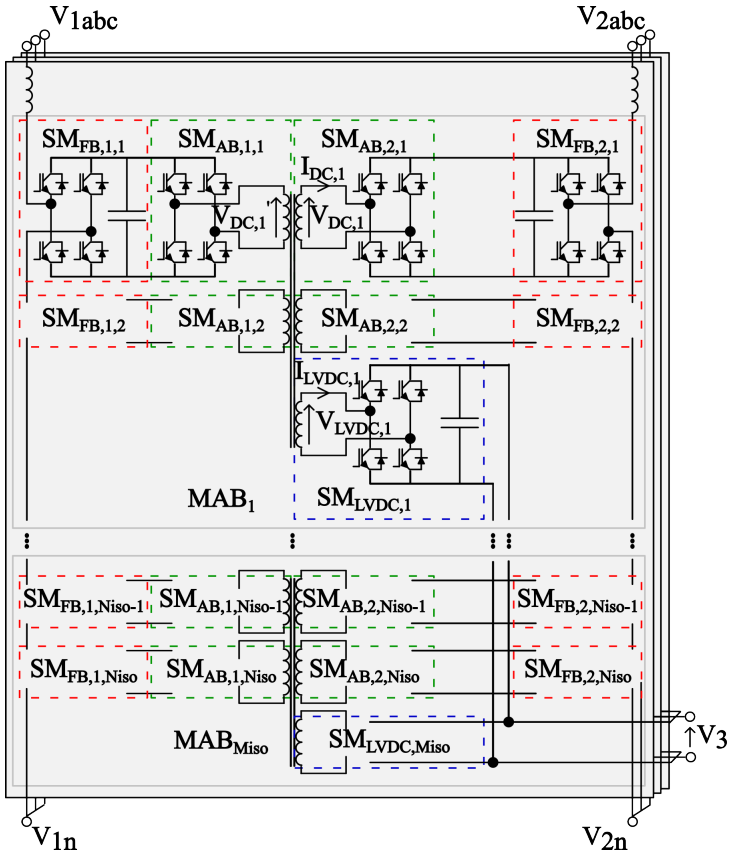


Figure 9: Isolated topology winner: Cascaded H-bridge with multi multi-active bridge.

$\hat{V}_{AC}$ is the peak line-line AC voltage and $V_{SM,FB}$ is the voltage blocking capability (considering switch utilization) of the FB switches. To generate a given intermediate DC voltage V_{MVDC} an additional set of $N_{P.Iso,DC}$ SMs is required per phase of the MMC

$$N_{P.Iso,DC} = ceil(\frac{V_{MVDC}}{V_{SM,FB}}) \tag{2}$$

The lower the modulated intermediate DC voltage the lower the number of MMC SMs required. A non-zero intermediate DC voltage is required to offer the connection point for the ISOP DC/DC converter.

Considering the two sets of identical three phase MMCs for the ESOP application (where $\hat{V}_{AC1} = \hat{V}_{AC2}$), $6N_{P.Iso} = 6(N_{P.Iso,AC} + N_{P.Iso,DC})$ FB SMs will be required for the partially isolated topology. Each FB SM SM_{FB} will include four two quadrant LF switches S_{FB} and one SM capacitor C_{FB}. Each MMC leg will require one filter inductor L_f (aggregated representation of upper and lower inductance). One intermediate DC capacitance C_{MVDC} is required to interface the back-to-back MMCs to the ISOP stage.

The number of components required for the back-to-back MMC stage of the partially-

isolated topology can be defined as $N\underline{o}C_{MMC}$

$$N\underline{o}C_{MMC} = 6[N_{P.Iso} * SM_{FB} + L_f] + C_{MVDC} = 6[N_{P.Iso} * (4S_{FB} + C_{FB}) + L_f] + C_{MVDC} \quad (3)$$

The FB switches S_{FB} must withstand $V_{SM,FB}$. If there is no DC power transfer each leg (and therefore series-connected FB SM) experiences half the AC phase current $0.5\hat{I}_{AC}$. The legs must also share the current $I_{DC,ph}$ associated with the power transfer from the AC side to DC side, which will be at most a third of the rated power of the AC port P_{AC}

$$I_{DC,ph} = \frac{P_{AC}}{3V_{MVDC}} = \frac{\hat{V}_{AC}\hat{I}_{AC}}{2V_{MVDC}} \quad (4)$$

The total current through each FB switch is $\hat{I}_{FB}$

$$\hat{I}_{FB} = 0.5\hat{I}_{AC} + I_{DC,ph} \quad (5)$$

$M_{P.Iso}$ DAB modules are required to interface the intermediate DC bus to the LV DC port. Each DAB module is assumed to have a fixed voltage blocking ability $V_{SM,AB}$. $M_{P.Iso}$ is a function of the intermediate DC voltage with respect to the active bridge's voltage blocking ability

$$M_{P.Iso} = ceil(\frac{V_{MVDC}}{V_{SM,AB}}) \quad (6)$$

Each DAB module includes two active bridge SMs $SM_{AB} = 2(4S_{AB} + T.W.)$, which is composed of active bridge switches S_{AB} and transformer windings $T.W.$, one transformer core $T.C.$, and one LV output capacitor C_{LVDC}.

The number of components that the ISOP DC/DC conversion stage requires is defined as $N\underline{o}C_{ISOP}$

$$N\underline{o}C_{ISOP} = M_{P.Iso}[2 * SM_{AB} + T.C. + C_{LVDC}] = M_{P.Iso}[2(4S_{AB} + T.W.) + T.C. + C_{LVDC}] \quad (7)$$

Assuming a $1:1$ turns ratio on the primary and secondary sides of the DAB transformers, the current flowing through the active bridge switches $I_{LVDC,AB}$ depends on their share of the power flowing between the intermediate DC bus and the LV DC port P_{LVDC}

$$I_{LVDC,AB} = \frac{P_{LVDC}}{M_{P.Iso} * V_{LVDC}} = \frac{I_{LVDC}}{M_{P.Iso}} \quad (8)$$

The lower the modulated intermediate DC voltage (via negative SM insertion by the FB MMC) the lower the number of SMs required in both the MMC and ISOP stage. However, for a given power transfer, a lower intermediate DC voltage will drive an increase in DC current $I_{DC,ph}$ and therefore associated losses. The power rating of the ESOP MPC based on the Anell specifications has a very low power rating that won't be significantly affected

by large modulation ratios, but consideration needs to be made when scaling up to larger power levels.

Another downside of large FB MMC modulation ratios is the increased number of negative SM voltages that are inserted. As the overmodulation increases:

- Circulating energy increases [18]
- The lower number of series components and injection of negative voltages can require higher switching frequencies and associated losses [10]

Overall the benefit of FB MMC overmodulation to lower the intermediate DC voltage needs to be optimized to balance all of these features. [11] finds that the benefit of a lower DC voltage for lower component numbers increases with larger switch voltage blocking capabilities. An optimal efficiency configuration was identified with MMC FB switches rated at $V_{SM,FB} = 3.3\ kV$ (switching at $f_{Sw} = 0.1:1\ kHz$) and ISOP active bridge switches rated at $V_{SM,AB} = 1.2\ kV$ (switching at $f_{Sw} = 15\ kHz$). The sizing study in this deliverable uses the same switch ratings.

Derivation of the Isolated Topology's Components The isolated topology uses two identical three phase CHBs to integrate the two MV AC ports. For a given FB switch voltage blocking capability, the CHB requires half the number of series SMs N_{Iso} to integrate an AC voltage. However, the CHB's SMs are directly connected with the active bridge SMs of the MAB modules, whose switches have to be operated at higher frequency and will therefore be rated to a lower voltage blocking ability. Accordingly, the number of series CHB SMs must be defined as a function of this active bridge voltage blocking ability

$$N_{Iso} = \frac{\hat{V}_{AC}}{V_{SM,AB}} \tag{9}$$

Each CHB SM is assumed to be identical to the partially-isolated FB SMs, however, would be able to utilize lower voltage rated FB switches.

Each CHB leg uses a filter inductor, which is also assumed to be equal to the aggregated filter inductor for each leg of the MMC.

Considering the equal rating of both AC ports, the number of components required for the two three phase CHBs is defined as $N\underline{o}C_{CHB}$

$$N\underline{o}C_{CHB} = 6[N_{Iso} * SM_{FB} + L_f] = 6[N_{Iso}(4S_{FB} + C_{FB}) + L_f] \tag{10}$$

The CHB FB switches experience the full AC phase current but similar to the MMC switches can switch at LF

$$\hat{I}_{FB} = \hat{I}_{AC} \tag{11}$$

Three sets of M_{Iso} MAB modules are required to interface the two sets of three phases of N_{Iso} CHB SMs to one another and the LVDC port. M_{Iso} is defined to ensure that the number of CHB SM pairs (connecting the two AC ports) are grouped with one LV DC assigned active bridge around a transformer core proportionally to the power rating of the AC and DC ports

$$M_{Iso} = ceil(\frac{N_{Iso}}{P_{AC}/P_{LVDC}}) \tag{12}$$

The number of MAB modules may also be varied away from the proportional power ratio for techno-economic reasons. For example, M_{Iso} could be increased to mitigate operational complexities associated with a large number of active bridges around a single transformer core or could be reduced to reduce the number of expensive transformer core components.

Each active bridge SM is assumed to be identical to those in the ISOP converter, including four active bridge switches and one transformer winding. The LV DC active bridges also require an output capacitor C_{LVDC}.

The number of components required for the multi-MAB isolated DC/DC stage is defined as $N\underline{o}C_{MMAB}$

$$N\underline{o}C_{MMAB} = 3[2N_{Iso} * (4S_{AB} + T.W.) + M_{Iso}(T.C. + 4S_{LVDC} + T.W. + C_{LVDC})] \tag{13}$$

The active bridge switches interconnecting the AC ports must withstand a share of the AC power transfer

$$I_{AB} = \frac{P_{AC}}{3N_{Iso}V_{SM,FB}} = \frac{\hat{V}_{AC}\hat{I}_{AC}}{2\hat{V}_{AC}} = 0.5\hat{I}_{AC} \tag{14}$$

The LV active bridge switches depend on the given active bridge's share of the LV DC power transfer and the LV DC voltage, which is assumed to be equal to the active bridge's voltage blocking rating

$$I_{LVDC,AB} = \frac{P_{LVDC}}{M_{Iso}V_{LVDC}} = \frac{I_{LVDC}}{M_{Iso}} \tag{15}$$

All of the active bridge switches must switch at high frequency.

Results: Case 1 Figure 10 exhibits the results of the component count for the ESOP Case 1. The number of components are pictured as a function of the intermediate DC voltage level. Only the partially-isolated topology's number of components varies with the modulated intermediate DC voltage. As the DC voltage increases the number of MMC SMs increases (from a baseline of $N_{P.Iso} = N_{P.Iso,AC} = 42$ for $V_{DC} = 0$) as does the number of ISOP DAB modules.

The isolated topology does not have an intermediate DC bus, hence the lack of impact on its number of components. Two configurations of the isolated topology are pictured. Both configurations require the same number of CHB SMs to interface the fixed AC voltage

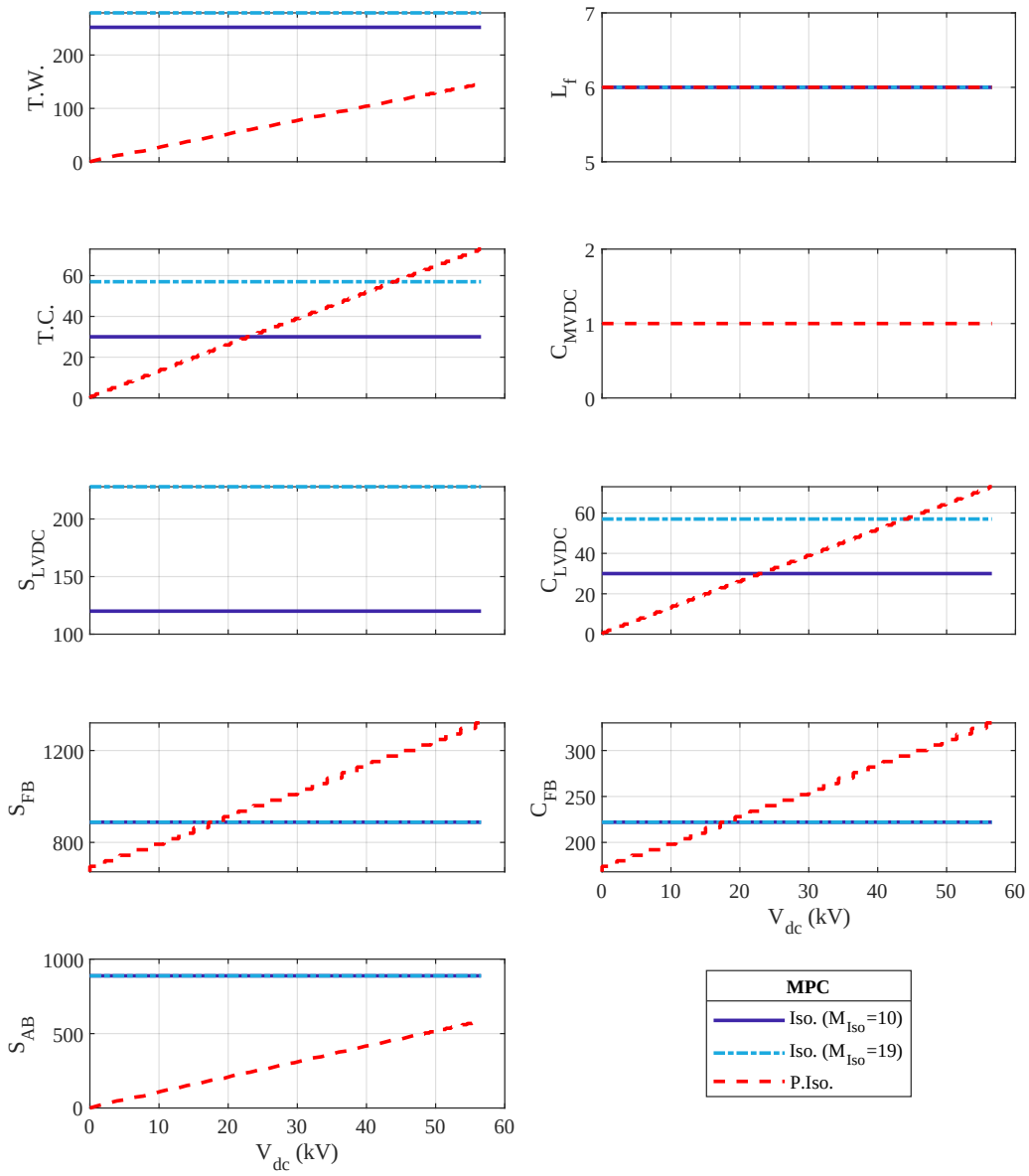


Figure 10: Comparison of component numbers for Case 1: 2x 20 kV AC DN ports and 1x 400 V DC ESS port.

($N_{Iso} = 37$), which is higher than the number of MMC SMs per arm for $V_{MVDC} = 0$ due to the constraint of the CHB SMs to the lower high frequency active bridge switch rating. One configuration has 10 MAB modules ($M_{Iso} = 10$), which is calculated to allocate the same ratio of CHB SM-linked active bridge pairs to LV DC port-linked active bridges as the AC to DC port power rating (using eq 12). This configuration of MAB modules groups four CHB SM-linked active bridge pairs (eight active bridges) with a single LV DC port-linked active bridge, resulting in nine active bridges around a single transformer core. A second configuration reduces the operational complexity associated with the high number of active bridges per MAB module by increasing the number of modules to $M_{Iso} = 19$ and therefore

reducing the number of active bridges per transformer core to five.

Both configurations of the isolated topology use a much larger number of transformer windings $T.W.$ and active bridge switches S_{AB} than any of the partially-isolated configurations. The partially-isolated topology uses identical active bridge switches on both primary and secondary sides of the ISOP DAB modules, hence the many more LV DC switches S_{LVDC} required for the isolated topology. The more operationally complex $M_{Iso} = 10$ isolated configuration has a lower number of transformer windings, transformer cores $T.C.$, LV DC switches, and LV DC capacitors C_{LVDC} than the less operationally complex $M_{Iso} = 19$ configuration.

The partially isolated topology may require an intermediate MV DC capacitor C_{MVDC} and also requires more FB switches S_{FB} and capacitors C_{FB} when operating with a high intermediate DC voltage. Two tipping points are shown in Table 3 where the partially-isolated topology moves below the $M_{Iso} = 10$ isolated topology in terms of component number: the first when the partially-isolated topology operates with an intermediate voltage of $V_{MVDC} = 22.62\ kV$ and the second when $V_{MVDC} = 17.16\ kV$.

At the lower tipping point the partially-isolated topology possesses a lower number of all components than the $M_{Iso} = 10$ topology. At the higher tipping point the partially isolated topology possesses a lower number of all components other than FB switches and capacitors. The partially-isolated topology's number of FB components is the most sensitive component-type to the intermediate DC voltage (despite their higher blocking ratio compared to the active bridge components) due to the two sets of three phase MMC legs that accelerate the increase.

Although it would be desirable to minimize the number of all components, the higher tipping point DC voltage level is deemed to be an acceptable operating characteristic due to the partially-isolated topology's low number of expensive transformer cores, lower number of LV DC capacitors, and significantly lower number of transformer windings, LV DC switches, and active bridge switches. The higher intermediate DC voltage will also achieve improved efficiency compared to a lower operating condition. The intermediate DC voltage $V_{MVDC} = 22.62\ kV$ requires a modulation ratio of $m = 2.5$, which fits within explored modulation ratios for similar two port applications (e.g. $m = 1.88 : 3.76$ in [18] and $m = 0.8 :> 5$ in [11]) and is therefore assumed to be feasible for the ESOP application. Additional work should explore the optimal modulation ratio to identify its impact on arm energy ripple (with impacts on SM capacitor sizing requirements) and circulating currents (with impacts on converter efficiency) as well as the number of components.

Results: Case 2 Figure 11 exhibits the results of the component comparison for ESOP Case 2, which includes lower AC port voltages $V_{AC} = 5\ kV$ and a higher LV DC port voltage

Table 2: Switch requirements for Case 1.

Component	Case	Switch Requirement							
		Partially-isolated				Isolated			
		V (V)	I (A)	f_{Sw}	Device	V (V)	I (A)	f_{Sw}	Device
S_{FB}	1	2145	15.94	LF	IGBT	780	16.33	LF	IGBT
	2		14.06						
S_{AB}	1	780	5.83	HF	SiC MOSFET	780	8.17	HF	SiC MOSFET
	2		4.42						
S_{LVDC}	1	*Identical to* S_{AB}				780	12.82	HF	SiC MOSFET
	2						6.75		

Table 3: Component count tipping points for Case 1.

Component	Number of Iso. Components (M_{Iso}=10)	V_{MVDC} (kV) when P.Iso. has fewer components
$T.W.$	252	Always
$T.C.$	30	22.62
S_{LVDC}	120	Always
S_{FB}	888	17.16
S_{AB}	888	Always
L_f	6	Always equal
C_{MVDC}	0	Never
C_{LVDC}	30	22.62
C_{FB}	222	17.16

$V_{LVDC} = 800\ V$. The higher DC port voltage doesn't impact the number of components of any of the topologies as it is assumed that a single active bridge switch can block the $V_{SM,AB} = 800\ V$.

The partially-isolated topology exhibits similar fundamental characteristics as for Case 1; requiring a higher number of components to support higher intermediate DC voltages. However, the lower AC port voltage can now be interfaced with a lower number of SMs (increasing from a baseline of $N_{P.Iso} = N_{P.Iso,AC} = 12$ for $V_{MVDC} = 0\ V$).

Also similar to Case 1, two isolated topologies are pictured, which both require a higher number of CHB SMs $N_{Iso} = 10$ compared to a single arm of the MMC (when modulating $V_{MVDC} = 0\ V$) due to the constraint of the CHB SMs to the active bridge voltage blocking ability. The number of MAB modules required is reduced compared to Case 1 due to the lower AC voltage. $M_{Iso} = 3$ represents the ideal configuration derived from eq 12 that groups four CHB SM-linked active bridge pairs proportionally to the number of LV DC port-linked active bridges according to the ratio of AC to DC port power (resulting in nine active bridges per transformer core). The number of active bridges per transformer core can now

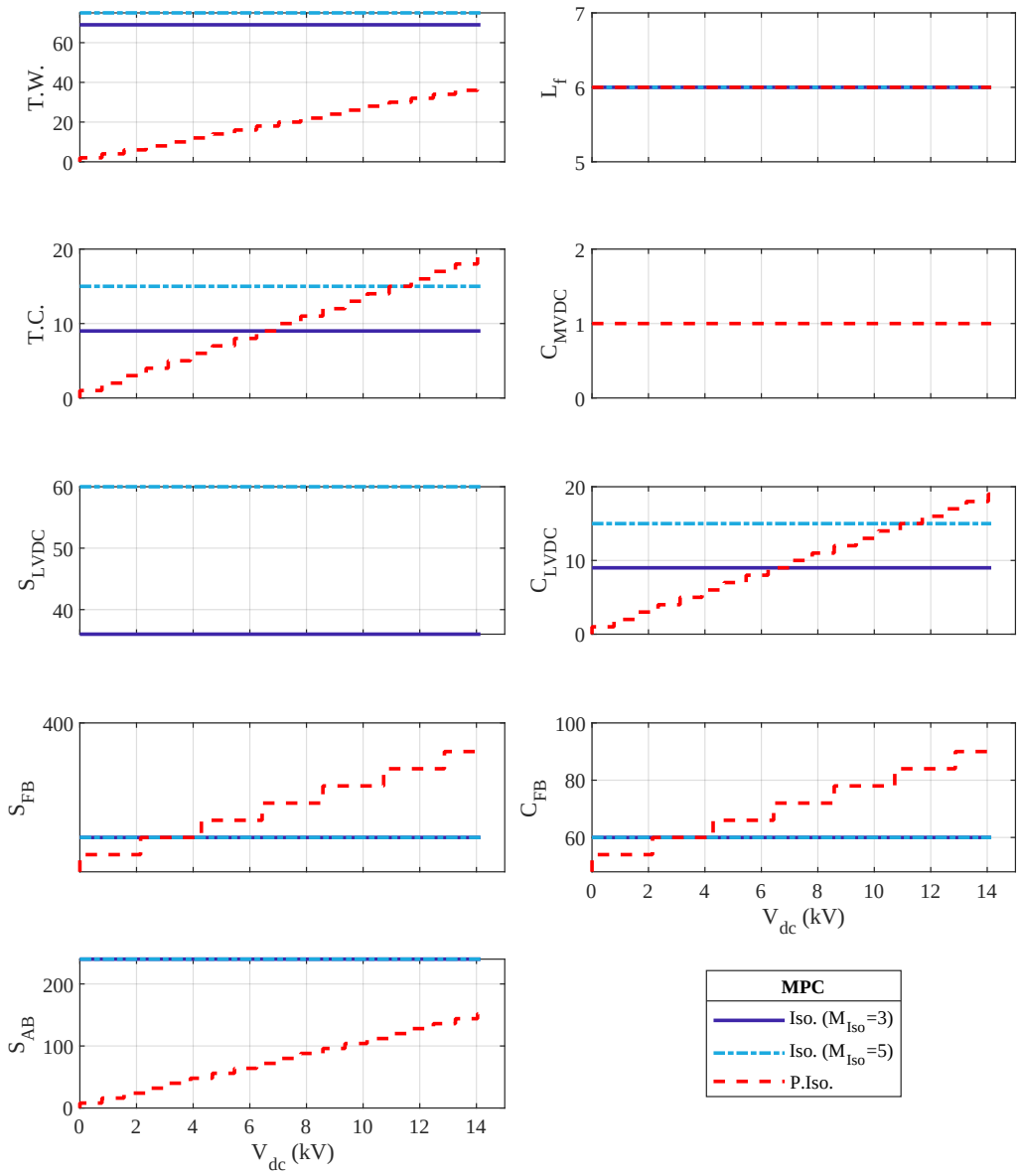


Figure 11: Comparison of component numbers for Case 2: 2x 5 kV AC DN ports and 1x 800 V DC ESS port.

be reduced to five by increasing $M_{Iso} = 5$.

The topologies exhibit similar relationships to one another as for Case 1 but now all topologies require a lower number of components (other than the fixed $C_{MVDC} = 1$ that could be sized lower for the lower intermediate DC voltages) due to the lower AC voltages. The two tipping points where the partially-isolated topology outperforms the $M_{Iso} = 3$ isolated configuration occur at $V_{MVDC} = 2.15\ kV$ and $V_{MVDC} = 6.24\ kV$ (detailed in Table 4). The higher tipping point operating condition again corresponds to a lower number of all components in the partially-isolated topology other than FB switches and capacitors.

The lower tipping point corresponds to a modulation ratio $m = 6.6$ while the higher

Table 4: Component count tipping points for Case 2.

Component	**Number of Iso. Components** (M_{Iso}=10)	V_{MVDC} (kV) **when P.Iso. has fewer components**
$T.W.$	69	Always
$T.C.$	9	6.24
S_{LVDC}	36	Always
S_{FB}	240	2.15
S_{AB}	240	Always
L_f	6	Always equal
C_{MVDC}	0	Never
C_{LVDC}	9	6.24
C_{FB}	60	2.15

tipping point corresponds to a modulation ratio $m = 2.3$. The difference in modulation ratio is exaggerated due to the larger impact of the switch voltage blocking abilities on the lower AC and intermediate DC voltage levels. The lower tipping point modulation ratio now exists beyond the upper limit of explored modulation ratios in the literature and is deemed to be undesirably large.

3.3.2 Qualitative Scoring of Topology Characteristics

The key operational characteristics of the two winning topologies for the ESOP MPC application are now compared in detailed. The characteristics are discussed in the following subsections before being qualitatively scored using a traffic light system (good/mid/poor) that is depicted in Figure 12.

The key characteristics for the ESOP application are:

- The impact of AC port, intermediate stage (MV DC bus or HF transformer), and LV DC port loss
- The impact of AC/DC converter and isolated stage component failure
- The ability to operate throughout unbalanced conditions
- Design flexibility and modularity
- Core coupling and control complexity

Port Fault Tolerance (Loss of Port or the Intermediate Stage) [24] (Chapter 5) explores the characteristics of a back-to-back MMC with DC load port in response to a range of port faults. The MMC is shown to be capable of riding through AC faults without passing critical fault dynamics to the intermediate DC bus but that the exact behavior of

the DC voltage, arm voltages, and total energy depends on the MMC's control approach. The FB MMC is shown to be capable of blocking a DC fault and therefore enabling continued AC STATCOM behavior when using crossed control. Active power could not be transferred between ports in the case of intermediate DC bus fault.

In the case of a LV DC port fault the ISOP DC/DC converter will likely need to be shutdown following the identification of a fault to reduce the transformer voltage to zero and de-energize the LV side [7]. The intermediate DC bus may be able to remain energized and support back-to-back operation of the MMCs without access to the LV DC port. This MPC fault operation requires additional analysis.

The performance of the isolated topology during different port faults is explored in [24] Chapter 4. [24] highlights that the loss of either AC port impacts the fundamental power flow through the link CHB SMs and active bridges and therefore requires fault identification and a control mode shift. However, the isolated topology simply views loss of the LV DC port as a DC load change. Although the intermediate transformer stage failure is unlikely it would result in shutdown of the entire MPC.

Component Failure Tolerance The partially isolated topology is resilient to MMC SM failure due to their ability to be bypassed. Additionally, the parallel components of the ISOP DC/DC stage offer redundancy. However, the ISOP stage will be sensitive to active bridge failure on the input-series side of the DC/DC converter.

The isolated topology is less resilient to CHB SM failure due to their direct linkage with the MAB SMs. The failure of these components will impact MAB power flow and SM balancing but is manageable due to the many redundant paths below rated operation. Failure of LV active bridge components shouldn't significantly impact the converter's capacitor balancing.

Performance in Unbalanced Conditions The partially-isolated topology's MMC can utilize circulating current, energy balancing, and negative sequence controllers to suppress the second harmonic current that results from unbalanced conditions [25]. These controls minimize the impact of unbalanced conditions on the intermediate DC bus and hence the MPC.

The isolated topology is sensitive to unbalanced conditions, where the coupling of all ports through the HF transformer can result in the transfer of power oscillations. Oscillations can be mitigated with the addition of negative sequence controllers [24] (Chapter 4).

Design Flexibility/Modularity The FB MMC of the partially-isolated topology is flexible to support different MV AC voltages either with the variation of the modular SMs or directly using a fixed configuration and varying the insertion of SMs. The flexibility of the FB MMC is particularly relevant in the case of an ESOP that interfaces two different AC voltage

levels, where either different MMC configurations can be used for the different ports or identical MMCs can be used with varying modulation ratios. The ISOP stage also has a relatively modular configuration that can be varied to support different intermediate DC voltage levels.

The CHB and multi-MAB isolated configuration also has the ability to be reconfigured for different voltage characteristics but will require significant rewiring to do so.

Core Coupling and Control Complexity The ports of the partially-isolated topology are all significantly decoupled due to the intermediate DC bus. Additionally, the distinct DAB modules do not interact with one another on the AC side, result in zero transformer core couplings between modules and relatively simple controllability.

In contrast, the MAB modules experience significant core couplings, which increase with the number of active bridges around a single transformer core. This can result in high control complexity.

3.4 Discussion and Conclusions

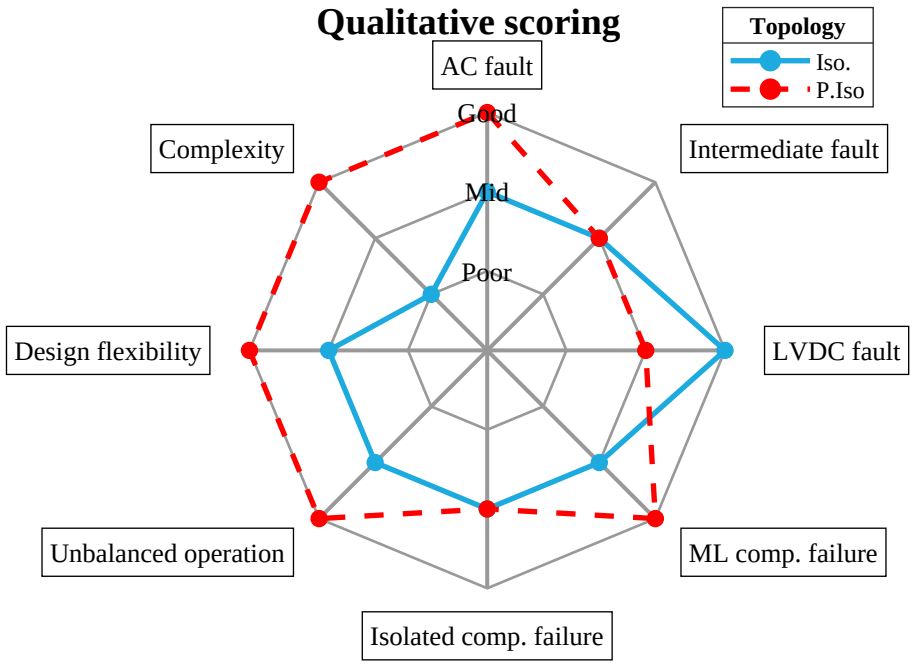


Figure 12: Comparison of qualitative feature scoring.

The component count provided an initial proxy to overview the cost and size of the two topologies for the two ESOP cases. The results showed that the partially-isolated topology becomes increasingly desirable as the intermediate DC voltage level decreases.

This is particularly true considering its lower dependence on expensive components such as transformer cores $T.C.$ and high frequency switches S_{AB}. Table 2 highlighted the low current utilization for the given application specifications at both of the DC voltage tipping points, which falls well within market-available switch specifications and highlights that both topologies may continue to be suitable for applications with power one or two orders of magnitude greater. The partially-isolated topology is expected to have a lower number of components than the more operationally complex isolated configurations even at the higher tipping DC voltage level (for both cases). This higher tipping point DC voltage level is suggested to be used as it maintains a lower MMC modulation ratio, which will maximize efficiency.

Although the component count analysis provides an initial comparison of topology cost and size, a more detailed analysis could be implemented. For example, the modulation ratio of the partially-isolated topology could be optimised with respect to the number of components, the impact on arm energy ripple and the circulating current, similar to the methodology for a two port application in [11].

Figure 12 pictures the qualitative scoring (either good, mid, or poor) of the topology characteristics, which is justified by the discussion in Section 3.3.2. The partially-isolated topology is only deemed to be outperformed by the isolated topology in the functional ability to handle LV DC port failure. Overall, considering the low component count of the partially-isolated topology for feasible intermediate DC voltage levels and its qualitatively determined superior performance, the partially-isolated topology is deemed to be most suitable for the ESOP MPC application and therefore is chosen to be pursued for laboratory verification.

4 Evaluation and Model-Free Optimization of Isolated DC–DC Triple-Active-Bridge Converters for MV Multi-port Converter Applications

In the previous Chapter, a qualitative comparison of various topologies have been made. One of the main components of the isolated topologies is a DC-DC converter based on DAB, TAB or MAB depending on the application. In this section, an optimization and evaluation of a TAB DC-DC converter is performed to demonstrate its application in MV multiport converters.

4.1 Introduction

Isolated multi-port converters (IMPCs) offer several potential advantages, including high efficiency, high power density, and galvanic isolation among the ports [31]. These merits are commonly attained by exploiting a multi-terminal high-frequency transformer (HFT) to facilitate interfacing ports with different voltage or current ratings [31]. IMPCs fit into several applications, such as DC microgrids and electric vehicles [32, 33]. The triple active bridge converter (TAB), displayed in Fig. 13 [34], is an IMPC with three ports, and it can be considered as an extension to an additional port of the dual active bridge (DAB) [35]. TAB comprises a three-terminal HFT connected to three bridges [34]. The HFT plays a crucial role in interfacing the DC ports and allowing a controlled energy transfer path through its leakage inductances $L_1 L_2$, and L_3 [34].

Phase shift modulation (PSM), represented in Fig. 14(a), can be utilized to control the power flow in TABs [34]. To this end, considering v_1 as a reference, PSM concerns the definition of the external phase shifts ϕ_2 and ϕ_3 of the generated ac voltages v_2 and v_3. PSM is a straightforward modulation scheme featuring low conduction losses and the capability to achieve zero voltage switching (ZVS) in some operating conditions. However, PSM operation may significantly depart from the optimal condition, where high losses emerge at low power transfer and/or when the voltage ratios of the ports are not matched with the transformer turns ratio, i.e., $V_2/V_1 \neq n_2/n_1$ and $V_3/V_1 \neq n_3/n_1$ [34]. Multiphase-shift modulation (MPSM), shown in Fig. 14(b), was introduced to overcome PSM limitations by exploiting internal phase shifts too, namely the duty-cycles D_1, D_2, and D_3 of the voltages v_1, v_2, and v_3, respectively [34]. MPSM allows tuning TAB operation by adjusting these duty-cycles aiming at operating points with reduced rms and full ZVS operation.

While optimizing the operating efficiency is the overarching objective [34, 36–44], securing ZVS operation throughout the entire range of operation also presents remarkable advantages, including the following:

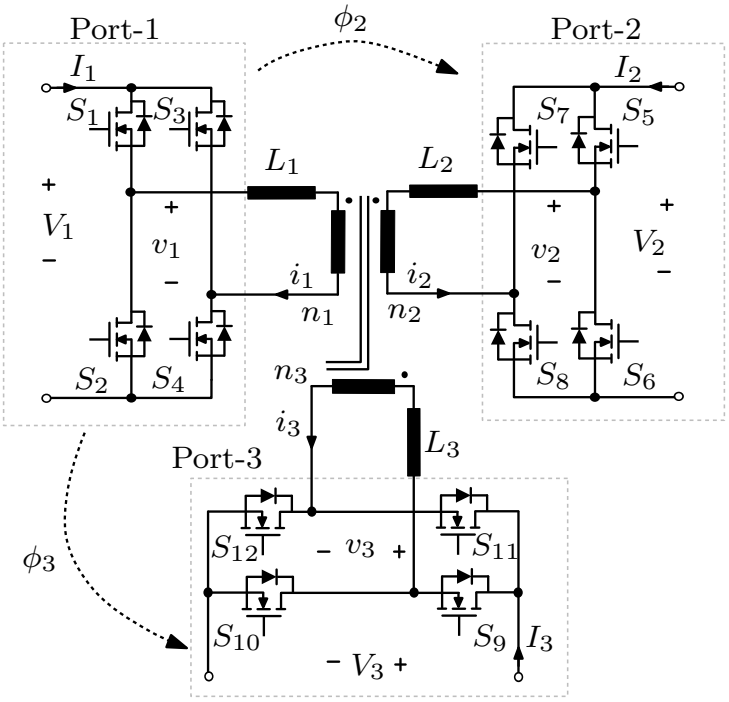


Figure 13: TAB converter

1. **Enhanced efficiency at high switching frequencies:** The utilization of wide-bandgap semiconductors (i.e., SiC, GaN) elevates the switching frequency, reducing the size of the passives [45]. However, switching losses have a higher impact at higher switching frequencies. ZVS abates turn-on losses of the switches, which is a significant part of the switching loss [45].

2. **Improved reliability:** Reduced switching loss means that devices are subjected to less thermal stress. Additionally, ZVS helps prevent undesired voltage ringings, which are also associated with reduced component stresses and overall better reliability [46].

3. **Reduced EMI:** ZVS ensures, by definition, soft switching transitions, which are associated with lower generated electromagnetic noise [47].

4. **Lessen snubber circuit requirements:** TAB operation can be exploited to achieve ZVS over the whole operating range by a proper modulation scheme [45].

ZVS conditions of TABs have been discussed in several works. In [36], a ZVS criterion that considers all TAB parameters has been introduced, but neglecting conduction losses. Alternatively, [37] established a universal analytical model for the TAB using a frequency domain analysis, accompanied by a particle swarm algorithm that minimizes rms current while meeting ZVS constraints. Despite their efficacy, the optimizations introduced in [36] and [37] rely on complex analytical models of TAB and, due to the use of given look-up tables, they lack the flexibility to adapt to the actual hardware and operating conditions.

In the following, a model-free online optimization for TAB based on multi-dimensional

ripple correlation control (MD-RCC) is proposed. MD-RCC has been applied to optimize the rms current of TAB in [44] and the efficiency of the QAB in [48]. However, this method is originally applied herein to optimize ZVS and reduce rms current, which also allows valuable converter performance in terms of overall conversion efficiency. The proposed approach offers both online and model-free advantages, allowing for online adaptation to potential parameter changes such as resistances, inductances, deadtime, switching frequency, etc.

4.2 Optimal Modulation of TAB Converters

PSM is a straightforward modulation scheme employed to regulate the power flow in TABs, as shown in Fig. 14(a). By the PSM, the external phase shifts, ϕ_2 and ϕ_3, between the three bridges, considering the first bridge as a reference, are adjusted to control the power flow, directing it from the leading to the lagging port, with the theoretical maximum at a phase shift of $\pi/2$ [34]. The external phase shift ϕ_2 represents the displacement between the switching of S_1 and S_5, likewise ϕ_3 is the shift between S_1 and S_9, as shown in Fig. 14(a). However, PSM leads to high losses, especially with low transferred power and mismatches among the ports voltage ratios and the transformer turns ratio. This brings increased rms current, increasing joule losses, as well as loss of ZVS. Instead, by MPSM, the internal phase shift between two legs within a full bridge is controlled beside the external phase shifts in order to alleviate the issue [34]. The internal phase shift for each bridge is represented by the duty-cycle of the corresponding bridge, namely, D_1, D_2, and D_3 for the three bridges, as shown in Fig. 14(b). The internal phase shift represents the shift between the switching instances of S_1 and S_4 for port-1, controlling D_1, as shown in Fig. 14(b); analogously for port-2 and 3.

4.2.1 Optimizing MPSM for Minimum rms Current

With the additional degrees of freedom, namely, D_1, D_2, and D_3, improved TAB operation can be obtained. In [41–44], the pursuit of minimizing the joule losses involves reducing the rms currents flowing through the converter, pursued herein by the measure (16).

$$i^{rms} = \sqrt{\sum_{n=1}^{3} i_{n,rms}^2} \tag{16}$$

To show the effectiveness of MPSM over PSM, a grid search optimization (GSO) is carried out to determine the optimum duty-cycles (i.e., D_1, D_2, and D_3) for minimum total rms current. The GSO systematically explores all possible combinations of duty-cycles for a TAB converter with parameters outlined in Table 5, using a PLECS simulation. Meanwhile,

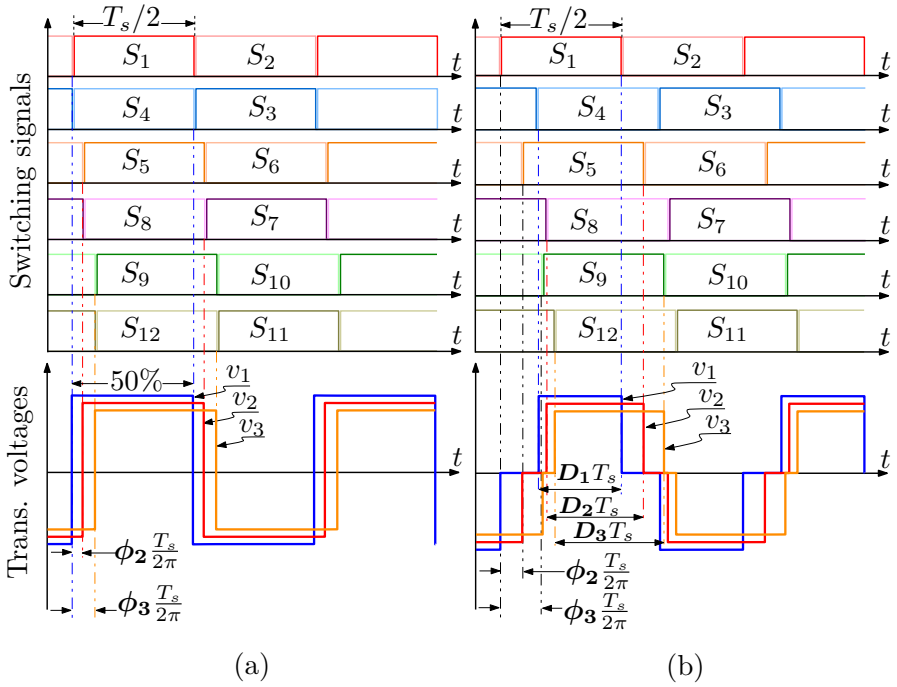


Figure 14: Switching sequence of TAB modulation schemes: (a) phase-shift modulation (PSM); (b) multiphase-shift modulation (MPSM).

the phase shifts (i.e., ϕ_2 and ϕ_3) are adjusted using a pair of regulators to control the power exchange at port-2 and port-3. The simulation is designed to consider various loading conditions. Port-1 and 2 voltages remain constant at their rated values, while port-3 voltage varies from 0.6 to 1.4 the rated voltage. In this setup, the power flows from port-1 to ports-2 and 3. Port-2 power is constant at 100, while port-3 power changes from 100 to the rated power. The GSO is employed with a resolution step of 0.05 on the duty-cycles.

Fig. 15(b) shows that the rms current by the GSO is reduced as compared to Fig. 15(a). The recorded reductions score up to 80% of the original value with the PSM. Such a substantial decrease in total rms current is particularly valuable in scenarios of low-power operation with voltage mismatch.

4.2.2 Optimizing MPSM for Enhanced ZVS and Reduced rms Current

To compare the effectiveness of different modulation schemes in achieving ZVS, criteria to discern ZVS should be defined first. As detailed in [49], the criteria used herein is based on the computation of the minimum threshold current i_{th} necessary to discharge the parasitic capacitance C_{eq} of a switching device initially operating at voltage V_{ds} and assuming a fixed discharge current during a given available deadtime $t_{deadtime}$:

$$i_{th} = \frac{2V_{ds}C_{eq}}{t_{deadtime}} \tag{17}$$

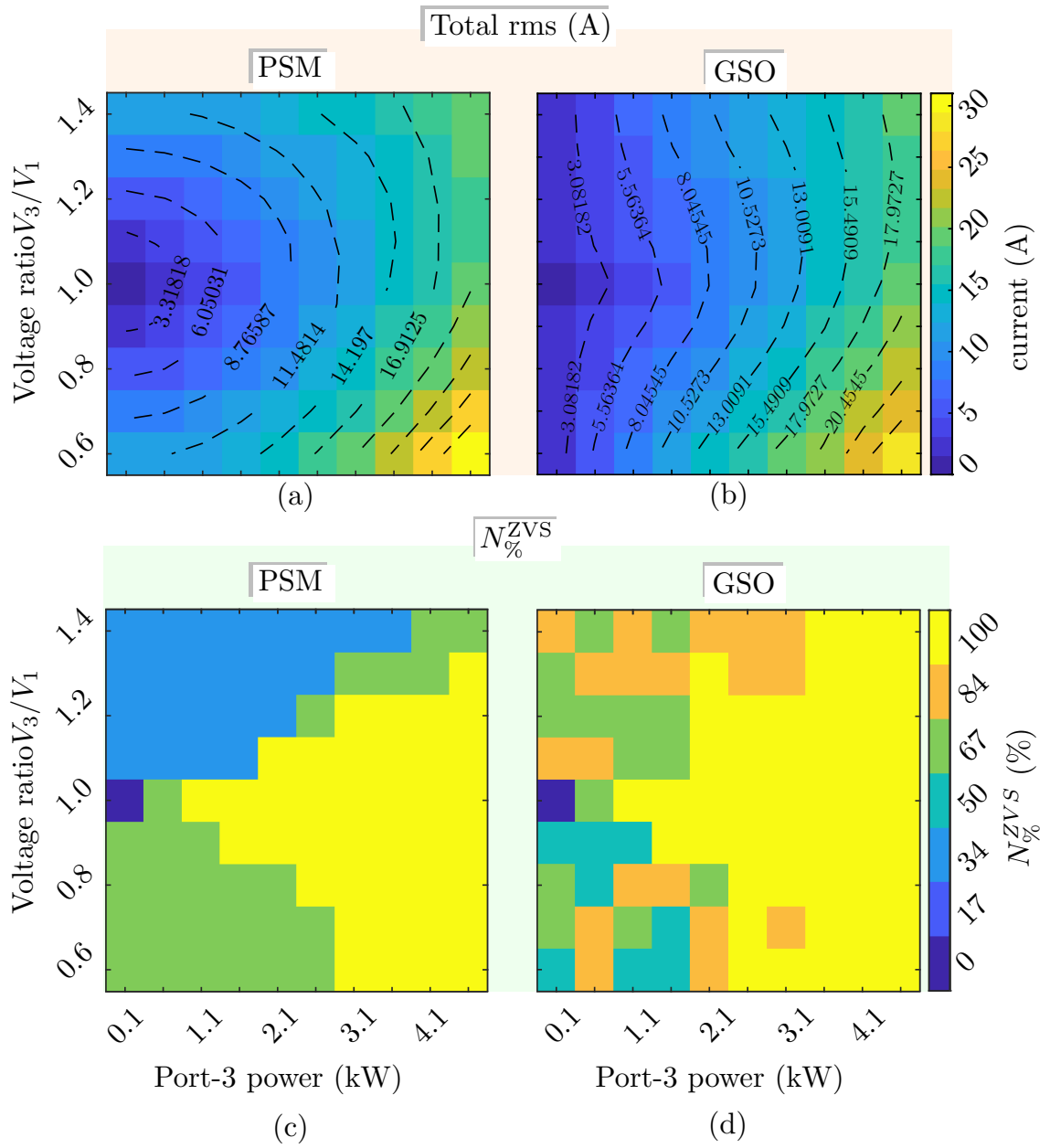


Figure 15: Simulation results of TAB; (a)-(b) total rms current for PSM and GSO, respectively; (c)-(d) percentage of devices achieving ZVS ($N_{\%}^{\mathrm{ZVS}}$) for PSM and GSO, respectively. Converter parameters as in Table 5 of Sec. 4.4.

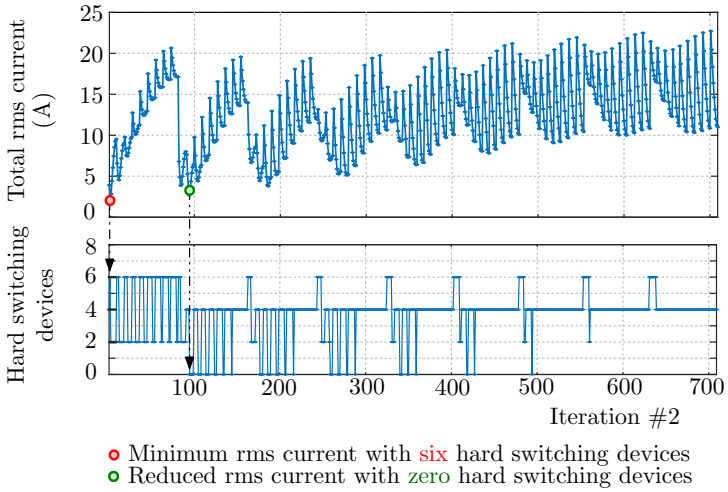


Figure 16: Total rms current and the corresponding number of hard switching devices for each iteration of GSO.

For example, considering the parameters in Table 5, the calculated threshold current is 400. For a single leg comprising two switches, namely S_1 and S_2, as illustrated in Fig. 13, with current and voltage directions indicated, the ZVS conditions are as follows.

1. The upper switch S_1 achieves full ZVS if the turn-on current i_{S1_on} is less than the negative threshold value, that is, $i_{S1\_on} < -i_{th}$.

2. The lower switch S_2 achieves full ZVS if the turn-on current i_{S2_on} is greater than the positive threshold value, that is, $i_{S2\_on} > +i_{th}$.

Based on these conditions, the percentage of devices satisfying the ZVS criteria is assessed and referred to as $N_{\%}^{\text{ZVS}}$. The results are illustrated in Fig. 15(c) for PSM and in Fig. 15(d) for GSO referring to (16). It is worth mentioning that the GSO objective is exclusively to identify points with the lowest rms current, regardless of ZVS conditions. Consequently, the attained ZVS profiles are incidental.

To show that operation with all transitions in ZVS can be reached with MPSM, the GSO is modified to search for minimum rms current restricted within the subset in which full or partial ZVS is realized. Fig. 16 displays the GSO iterations for the test case in Fig. 15 with port-3 power at 100 and port-3 voltage at 240. For the GSO aiming to minimize the rms current only, iteration #2 gives the best outcome, yielding a total rms current of 2.17 with six devices in hard-switching, that is, $N_{\%}^{\text{ZVS}} = 50\%$. Differently, when integrating ZVS as a requirement for the GSO solutions, iteration #95 yields a total rms current of 3.26 with zero hard switching devices, achieving 100% ZVS.

Noticeably, pursuing minimum rms current within a subset featuring all the transitions in ZVS might lead to an increase in the total rms current. However, this outcome is also dependent on the GSO resolution step: a finer step could potentially locate better solutions

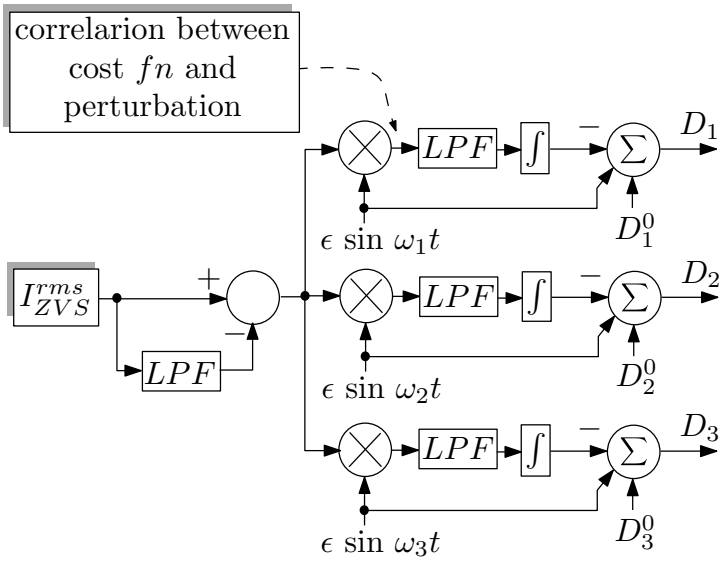


Figure 17: Multi-dimensional ripple correlation search (MD-RCC).

with lower rms currents. Additionally, even with the modified GSO, the obtained rms current still demonstrates a significant reduction as compared to the PSM marked at approximately 11.

4.3 Online Model-Free Optimization of TAB

In Sect.4.2, MPSM shows the ability to attain full or partial ZVS and reduce the flowing rms currents. However, the employed GSO exhibits drawbacks, including a substantial time requirement for data collection, a significant computational burden with a small resolution step, and the necessity to store results in look-up tables. Additionally, the GSO lacks the adaptability to accommodate parameter changes in the converter resulting from variations in operating conditions. Hence, an online model-free optimization method has been implemented to optimize the performance of the TAB with full or partial ZVS operation and with reduced rms currents. The optimization approach utilized herein is known as multi-dimensional ripple correlation control (MD-RCC), initially introduced in [44] to optimize the rms current of the TAB converter and in [48] to optimize the efficiency of the QAB. However, its application to optimize the ZVS operation of TAB has not been explored previously.

MD-RCC is based on the operating principle of the ripple correlation control (RCC), also known as extremum-seeking control (ESC) [50]. In RCC, the optimization of a specific cost function involves imposing a perturbation on the control variable. The correlation between the applied perturbation and the cost function is then identified. Subsequently, the control variable is adjusted, guided by the estimated correlation, in the direction of either maximizing or minimizing the cost function. In order to optimize a given cost function with multiple degrees of freedom, *corresponding* perturbations are superimposed on the control variables, herein duty-cycles D_1, D_2, and D_3. These perturbations must possess

distinct frequencies. This allows for independently measuring the correlation between the cost function and each perturbation, thanks to the orthogonality among the perturbations and the corresponding effects. The imposed perturbations can be defined as

$$\epsilon \sin \omega_p t, \quad p = 1, 2, 3 \tag{18}$$

Fig. 17 shows the implementation of MD-RCC. The low-pass filters (LPF) serve as an approximation of the moving average. Consequently, these filters should be designed with a cutoff frequency sufficiently lower than the minimum perturbation frequency. Additionally, the stability considerations in [44] must be considered:

1. The maximum perturbation frequency should be much slower than the plant dynamics (i.e., the plant is considered as a static map w.r.t the maximum correlation perturbation).
2. The perturbation frequencies should be different to guarantee orthogonality.
3. The low pass filters should have a cutoff frequency lower than the lowest difference between the perturbation frequencies.
4. The perturbation magnitude should have a very small value compared to the possible optimum (e.g., 1% of full duty-cycle).

To simultaneously maintain low rms currents and optimize ZVS operation, a novel cost function is introduced herein:

$$I_{ZVS}^{rms} = K_{rms}.i^{rms} + K_{ZVS}.\sqrt{\sum_{n=1}^{n_{\text{device}}} H.I_{n,HS}^2} \tag{19}$$

where, K_{rms} and K_{ZVS} are weighting factors—selected through iterative tuning to achieve the best trade-off between minimizing rms current and ensuring effective ZVS operation—i^{rms} is the total rms current as defined in (16), n is the number of switches ($n = 1, \ldots, 12$), H indicates whether the device is hard or soft switching, specifically, $H = 1$ for hard switching devices (i.e., ZVS criteria are not met), $H = 0$ for soft switching devices, and $I_{n,HS}$ denotes the switched current at the switching instant. The online computational procedure of $I_{n,HS}$ is shown in Fig. 18. The cost function includes the overall rms current of the TAB, combined with the hard switching commutation currents.

4.4 Simulation Results

To evaluate the effectiveness of the defined cost function, the MD-RCC-based approach was implemented in a simulation model using PLECS, with parameters listed in Table 5. The test

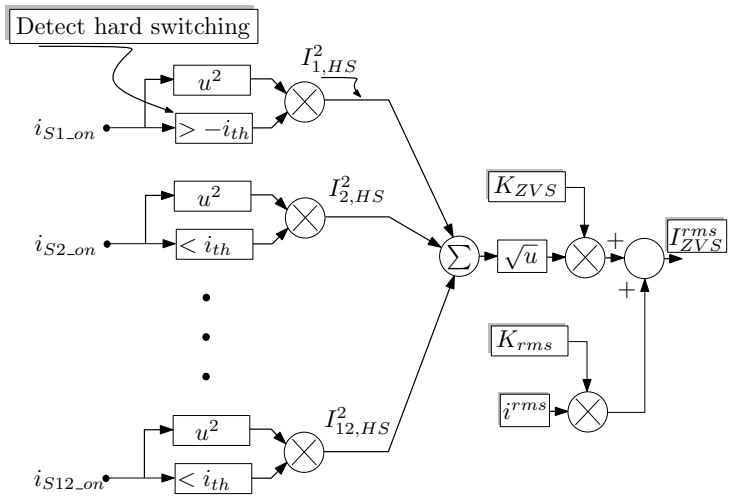


Figure 18: Hard switching current detection algorithm of the TAB in Fig. 13; i_{th} calculated with (17).

Table 5: TAB parameters.

Parameters	**Value**
Nominal power at each port P_{rated}	5
Switching frequency $f_s = 1/T_s$	40
Rated DC voltages V_1-V_3	400
Transf. turns ratio $n_1 : n_2 : n_3$	1:1:1
Transf. leakage inductances $L_1 - L_3$	44
Switching Devices	Cree C2M0080120D
Dead time	0.2
Sinusoidal perturbation magnitude ϵ	0.0025
Weights K_{rms}, K_{ZVS}	5, 10
Perturbation frequencies ω_1-ω_3	/ 10π, 14π, 18π,

scenario in Sect. 4.2 was considered to assess the optimization capability of the approach and the defined cost function in achieving ZVS for all the switches over a comprehensive set of operating conditions. For each combination of port-3 power and voltage, the MD-RCC is executed to minimize the proposed cost function (19), which takes into account both total rms current and the hard switching currents if ZVS criteria defined in Sect. 4.2.2 are not satisfied. This process steers the converter operation away from unfavorable operating conditions for ZVS while sliding towards operating points with low rms currents.

Fig. 19 shows the results of applying the MD-RCC considering the minimization of the total rms current i^{rms} (16) *versus* the proposed cost function I_{ZVS}^{rms} (19). As compared to rms currents minimization displayed in Fig. 19(a), the use of the proposed cost function leads to approximately equivalent rms currents in Fig. 19(b). However, by the proposed cost function, nearly all the switches satisfy the ZVS criterion, as shown in Fig. 19(d). This desirable result is not achieved using (16), as shown in Fig. 19(c), because such a cost function disregards switching conditions (i.e., soft or hard switching).

4.5 Experimental results

An experimental prototype has been developed with the parameters listed in Table 5. The experimental prototype is displayed in Fig. 20. To implement the cost function (19), an NI PXIe-1082 has been employed to oversample the HFT currents. The B-box RCP is utilized to control the Imperix power modules and to execute the proposed MD-RCC. A power analyzer PW8001 by Hioki has been utilized to monitor TAB efficiency and losses.

To validate the performance of the proposed optimization, several operating conditions have been considered. Herein, a test case is shown at which power is transferred from port-1 to ports-2 and 3, with $V_1 = 400$, $V_2 = 280$, $V_3 = 320$, $P_2 = 100$, and $P_3 = 600$. This test case is chosen at a low power level and with voltages mismatched to the transformer turns ratios to demonstrate the advantage of the proposed optimization in a relevant operating condition.

Fig. 21(a), (b), and (c) illustrate the dynamic response of the proposed MD-RCC optimizing only the total rms current i^{rms} (16). Fig. 21(a) shows the duty-cycles optimization aimed at minimizing i^{rms}, as shown in Fig. 21(b). The MD-RCC reduces the total rms current from approximately 7.5 at initial steady-state to about 5.5 at final steady-state, achieving a reduction of approximately 27% from the initial value. However, optimizing considering the total rms current solely does not ensure soft switching operation, as highlighted in Fig. 21(c): the sum of the hard-switching currents is reduced but not zeroed, indicating that hard-switching devices are still present.

Fig. 21(d), (e), and (f) illustrate the dynamic response of the proposed MD-RCC when optimizing I_{ZVS}^{rms} as defined in (19). The optimization goal of the MD-RCC is to minimize the

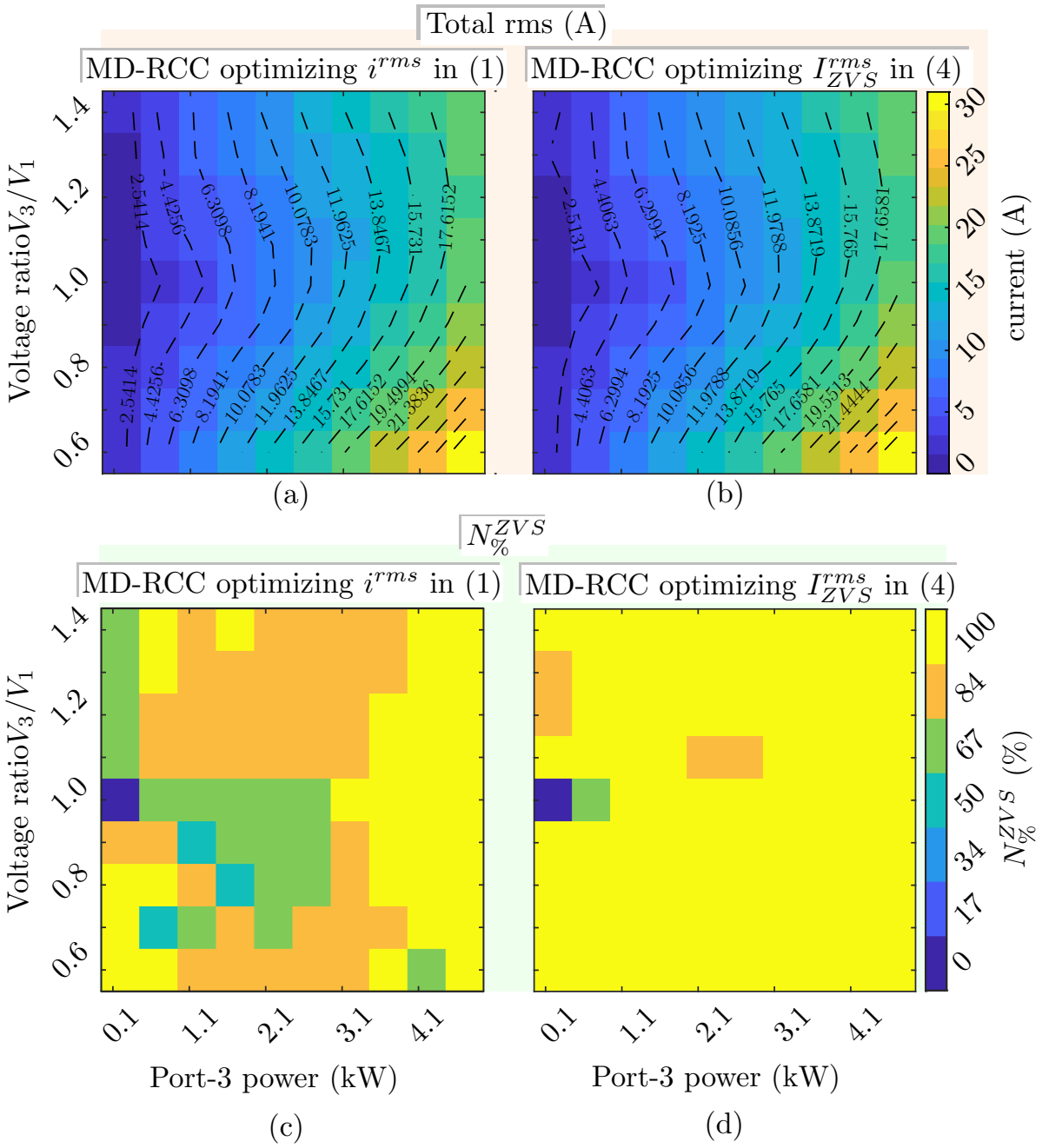


Figure 19: Simulation results of MD-RCC with TAB: (a)-(b) total rms current of MD-RCC optimizing i^{rms} in (16), and I_{ZVS}^{rms} in (19), respectively; (c)-(d) percentage devices achieving ZVS ($N_{\%}^{ZVS}$) of MD-RCC optimizing i^{rms} in (16), and I_{ZVS}^{rms} in (19), respectively.

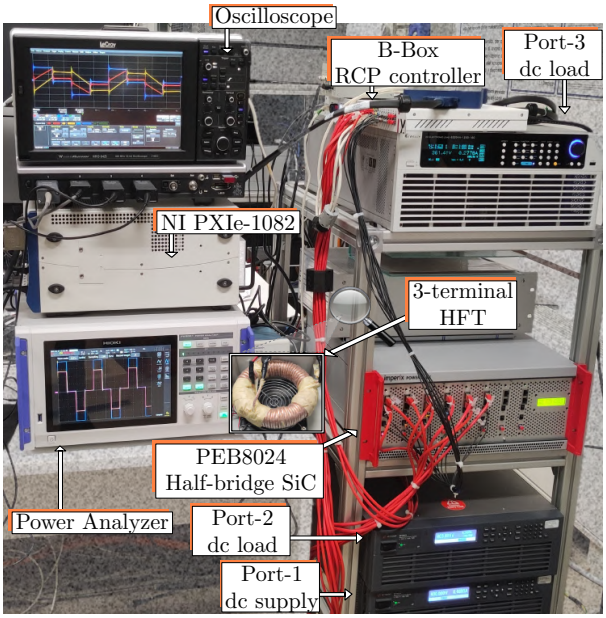


Figure 20: TAB experimental prototype.

combination of both the total rms current, as shown in Fig. 21(e), and the hard switching current, as depicted in Fig. 21(f).

Fig. 21(e) indicates a reduction in the total rms current, comparable to the reduction observed in Fig. 21(b). However, because the cost function I_{ZVS}^{rms} includes the hard switching current as an optimization target, Fig. 21(f) shows a reduction of the hard switching current, which is zeroed in steady state, indicating the elimination of hard switching devices by the end of the optimization process.

Fig. 22 shows the steady-state voltage and current waveforms of the HFT. Fig. 22(a) shows the waveforms at the initial state, where 8 switching devices have hard turn-on transition, indicated by red dots for ports-2 and 3. Fig. 22(b) shows the steady-state waveforms after optimizing i^{rms} (16), a reduction in the total rms current is evident. However, 4 switching devices remain in a hard turn-on transition, as shown for port-2. Fig. 22(c) illustrates the steady-state waveforms after optimizing I_{ZVS}^{rms} (19). The total rms current is reduced compared to the initial state, with complete soft switching transitions achieved for the three active bridges of the converter.

4.6 Conclusion

This section demonstrates the feasibility of achieving a trade-off between zero voltage switching (ZVS) operation and reduced rms current for the triple active bridge converter (TAB). Initially, a comprehensive grid search optimization (GSO) is employed to find the minimum rms current within a subset of points that achieve either partial or full ZVS. Subsequently, a multi-dimensional ripple correlation control (MD-RCC) is utilized to optimize

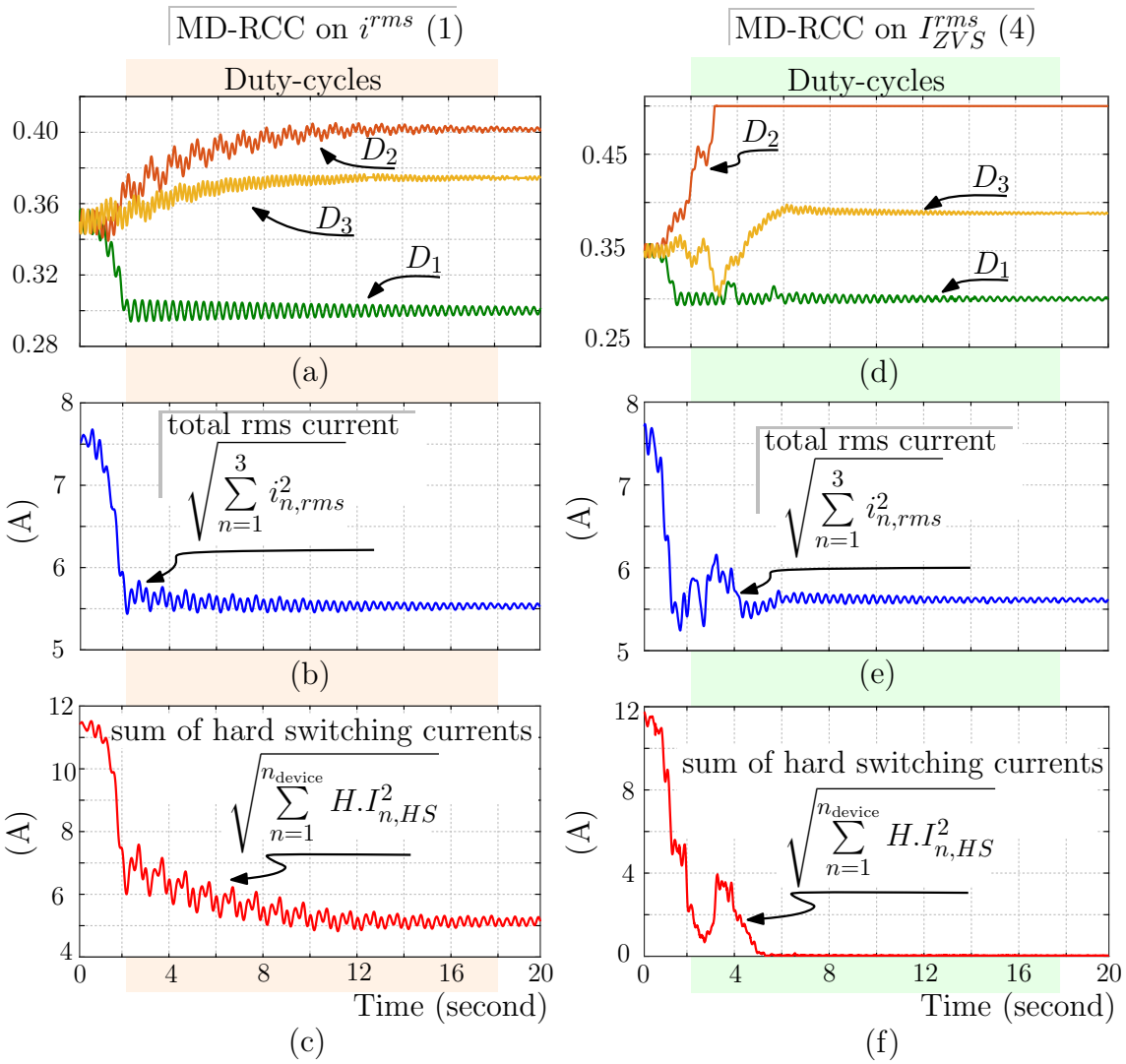
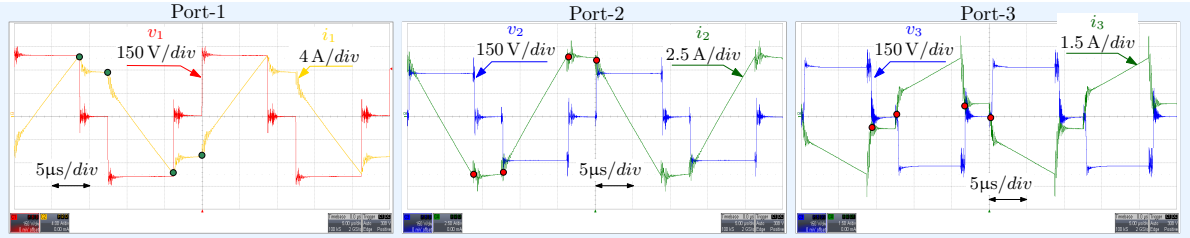
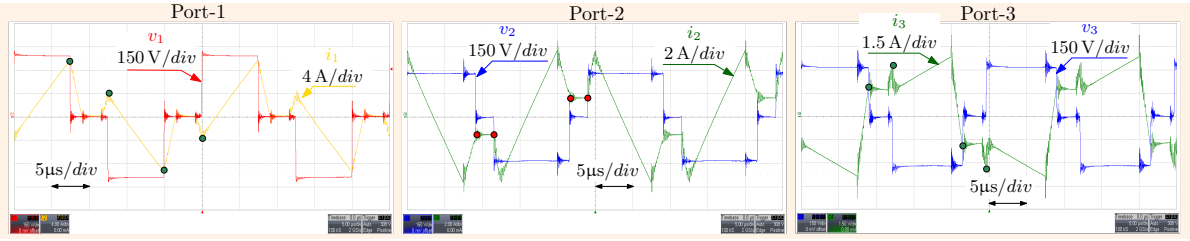


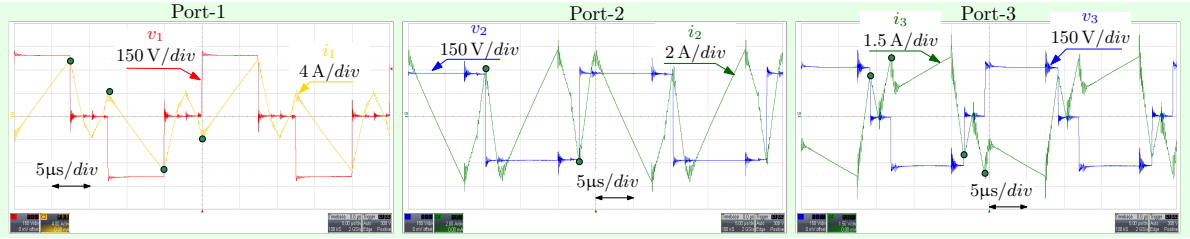
Figure 21: (a), (b), and (c) dynamic response of MD-RCC optimizing i^{rms} (16) : (a) duty-cycles; (b) total rms current; (c) sum of hard switching current; (d), (e), and (f) dynamic response of MD-RCC optimizing i_{ZVS}^{rms} (19): (d) duty-cycles; (e) total rms current; (f) sum of hard switching current.



(a) Initial state: total rms = 7.5 A, total hard switching current = 11.8 A, hard switching devices = 8.



(b) MD-RCC optimizing i^{rms}: total rms = 5.5 A, total hard switching current = 5.1 A, hard switching devices = 4.



(c) MD-RCC optimizing I_{ZVS}^{rms}: total rms = 5.6 A, total hard switching current = 0 A, hard switching devices = 0.

soft turn-on transition hard turn-on transition

Figure 22: Transformer voltage and current steady-state waveforms of the test case in Fig. 21: (a) at the initial state; (b) after MD-RCC optimizing i^{rms} (16); after MD-RCC optimizing I_{ZVS}^{rms} (19) .

a novel cost function that accounts for both rms current and hard switching currents. The proposed optimization algorithm is also validated through extensive simulation and experimental test cases.

5 Switching models and CHIL tests in non-isolated MV-MPC

In the case of non-isolated MPC, the structure and the controller presented in Deliverable 2.1 are used. Its structure is defined in Fig. 23.

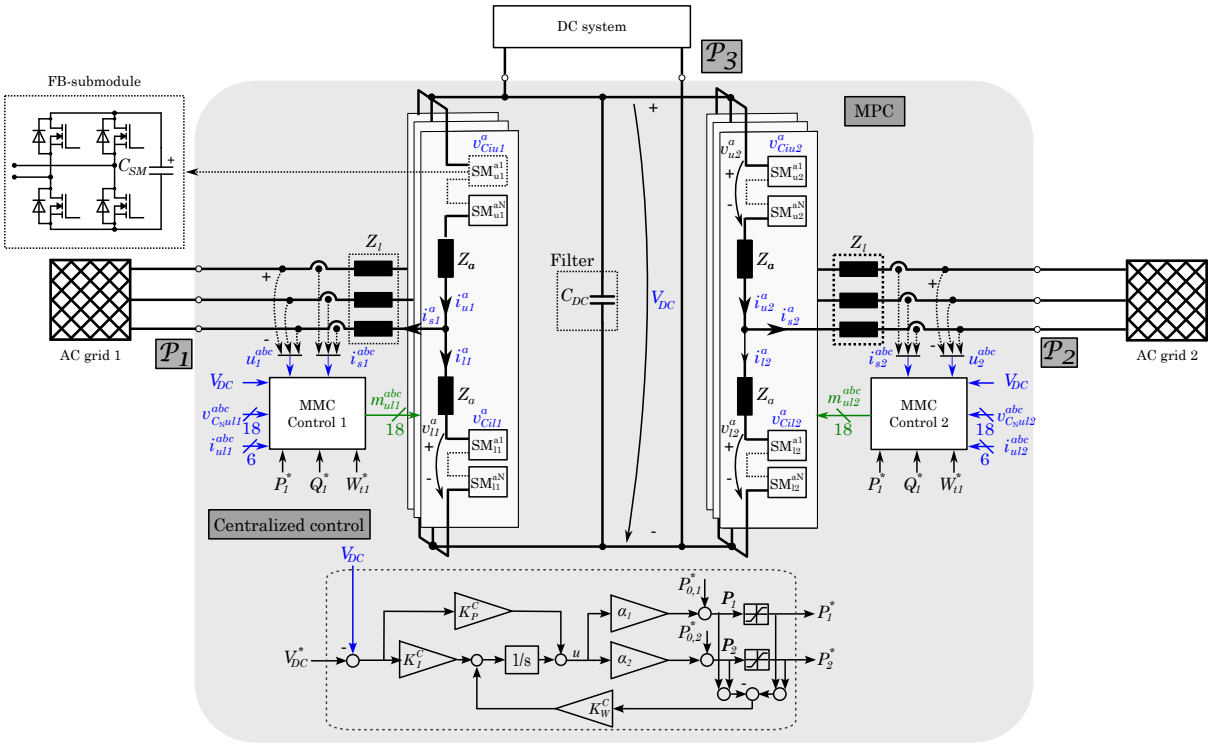


Figure 23: Topology and control of the studied topology.

In this section switching model and CHIL tests are done to demonstrate that the presented solutions could be used in real systems and to analyze the behavior of the system when the controller structure is changed.

5.1 Modulation

Since switching models are used in this deliverable, modulation is required. Various modulation techniques for MMCs are presented in the literature [26]. When there are many levels, Nearest Level Modulation (NLM) is the most effective option. However, an algorithm is necessary to balance the SMs. On the other hand, Phase Shifted Carrier (PSC) modulation is a technique that, while challenging to apply with a large number of levels, does not require an algorithm to balance the SMs [27]. Furthermore, another possible option is Space Vector PWM (SVPWM), but this technique becomes complex with more than three levels. Given that the designed MPC is intended for a MV application, PSC modulation is the selected technique. Due to the usage of FB-SMs, the phase shift of the carriers is critical to

reduce the addition of harmonics as a consequence of the modulation. Consequently, the carrier definition proposed in [28] has been used. In addition, as mentioned on Section II, a filter is added to delete the undesired harmonics that appear due to the modulation.

5.2 Outer loop comparison

For the analysis of AC and DC faults, switching simulations are performed using TyphoonSim. The controllers are defined as discrete, with a sampling time of 0.1 ms.

While averaged models are effective for control system studies, the dynamic effects introduced by IGBT switching must be considered for comprehensive system analysis. Therefore, the validation is done with switching models, even a large simulation time is required. HB-SMs could be used to handle AC faults, however, FB-SMs have been used in the simulation to ensure that the system could also operate with DC faults, without the use of a hybrid breaker.

The validation of both normal and fault operation of the MPC is conducted in a MV distribution grid. The investigated system has two feeders, with the MPC positioned at their endpoints. Load representation is omitted, as illustrated in Fig. 24. A meshed distribution network is analyzed due to its increased control complexity. Both balanced and unbalanced fault scenarios are examined, with particular emphasis on a severe fault occurring near one of the ports. Consequently, the port with the highest voltage margin prioritizes active current contribution to try to maintain DC voltage stability. This prioritization is enforced through both, current saturation and the centralized control algorithm.

Table 6: Model validation parameters

Parameter	**Value**
Controller sampling time, T_s	0.1 ms
Nominal AC grid voltage, V_{ac-N}	3.3 kV
Nominal port power, S_{c-N}	800 kVA
Nominal DC bus voltage of MPC, V_{dc-N}	6 kV
Short Circuit Ratio, SCR	10
R/X Ratio, R/X	1
Number of SMs per arm, N_{arm}	3
Sub-module capacitance, C_{SM}	10 mF
DC bus filter, C_{DC}, L_{DC}	1.59 μF
Modulation frequency, F_s	10 kHz
AC port active power references, P_1^*, P_2^*	-0.625 p.u., 0.5 p.u.
AC port reactive power references, Q_1^*, Q_2^*	0.375 p.u., -0.375 p.u.
DC voltage reference, V_{dc}^*	1 p.u.
DC Load active power reference, P_3^*	0.125 p.u.
Grid impedance, R_g, L_g	0.7R_{eq}, 0.7L_{eq}
Feeder 1 impedance, R_1, L_1	0.3R_{eq}, 0.3L_{eq}
Feeder 2 impedance, R_2, L_2	0.3R_{eq}, 0.3L_{eq}
Coupling impedance, R_l, L_l	0.01 p.u., 0.2 p.u.
Arm impedance, R_a, L_a	0.01 p.u., 0.2 p.u.

To validate the control behavior under normal and fault conditions, three different scenarios are considered:

- Scenario 1: A 3-port converter with two AC ports linked to the feeders and one DC port supplying a DC load, employing classical control. Only AC faults are applied.
- Scenario 2: A 3-port converter with two AC ports linked to the feeders and one DC port supplying a DC load, utilizing crossed control. AC and DC faults are applied.
- Scenario 3: A 3-port converter with two AC ports linked to the feeders and one DC port supplying a DC load, applying classical control to the port with the lowest voltage during the AC faults, while the other port operates under crossed control.

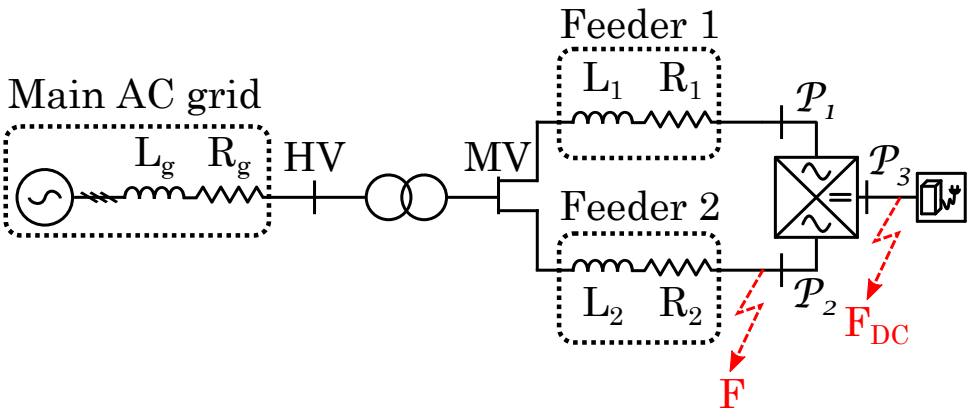


Figure 24: Scenarios considered for MPC control validation.

Scenarios 1 and 3 are tested under identical conditions. To verify correct controller performance under normal operation, the active and reactive power references are modified by 0.2 p.u. from their initial values. The robustness of the MPC control strategy is demonstrated by studying DC faults and balanced and unbalanced AC faults. Faults persist for 0.2 seconds in all test cases. The unbalanced faults presented in this study are single-phase-to-ground (Type B) faults, as classified in [29]. Although additional unbalanced fault types were tested, their results are omitted due to space constraints. In Scenario 2 a DC fault appears at $t = 7$ s and $t = 9$ s, during 0.2 s. With the first DC fault, no breaker is triggered, while during the second fault, after 20 ms breakers isolate the fault.

A time-domain simulation is conducted in TyphoonSim with the following key events:

- $t = 2$ s: Variation in MPC power.
- $t = 3$ s: Application of an unbalanced fault (F).
- $t = 5$ s: Application of a balanced fault (F).
- $t = 7$ s: Application of a DC fault (F_{DC}).

- $t = 9$ s: Application of a DC fault (F_{DC}) with breakers.

In Scenarios 1 and 3, only the total energy and the DC voltage are shown. In Scenario 2, additionally illustrated are the powers, to demonstrate the STATCOM behavior during DC fault. In the following section, while a CHIL validation is done, all the voltages, currents, powers and energies of the MPC are shown in detail, to demonstrate the correct behavior.

5.2.1 Scenario 1: Classical Control

This section analyzes a case in which both ports operate under classical control. DC faults are not addressed with this configuration, because, as discussed in Section III, classical control is unable to manage them effectively.

The results obtained in this Scenario are shown in Fig. 25.

Under unbalanced faults, total energy exhibit 100 Hz oscillations, which occur when the negative current reference is set to zero. In addition, for balanced faults, the total energy exhibits an initial peak but subsequently become stable, demonstrating that the proposed control strategy effectively regulates total energy using the zero-sequence additive current. During AC unbalanced faults, DC voltage remains controllable. In contrast, under balanced faults, DC voltage becomes unregulated and increases, even when the port with the largest voltage margin prioritizes active power injection.

From these results, it can be concluded that the classical control can handle unbalanced AC faults. However, with severe balanced AC faults, the classical control strategy successfully maintains total energy tracking, but at the expense of DC voltage regulation. Finally, the delay that appears due to the detection time affects the responses.

5.2.2 Scenario 2: Crossed Control

This section examines the same conditions as in Scenario 1, but with crossed control in the outer loops. In addition, a DC fault is evaluated in a three-port MPC to demonstrate that crossed control can, at a minimum, enable operation as a static compensator (STATCOM) under DC fault conditions.

The results of Scenario 2 time-domain simulation are represented in Fig. 26 and 27.

In this case, similar conclusions can be drawn regarding the 100 Hz oscillations that appear under unbalanced faults. During balanced faults, the total energy of the port closest to the fault becomes uncontrolled and decreases at a constant rate. In contrast, the DC voltage remains regulated, exhibiting smaller variations compared to the classical control.

These results demonstrate that the crossed control strategy effectively handles unbalanced AC faults. However, under severe balanced AC faults, while DC voltage remains controlled, proper regulation of total energy is not ensured.

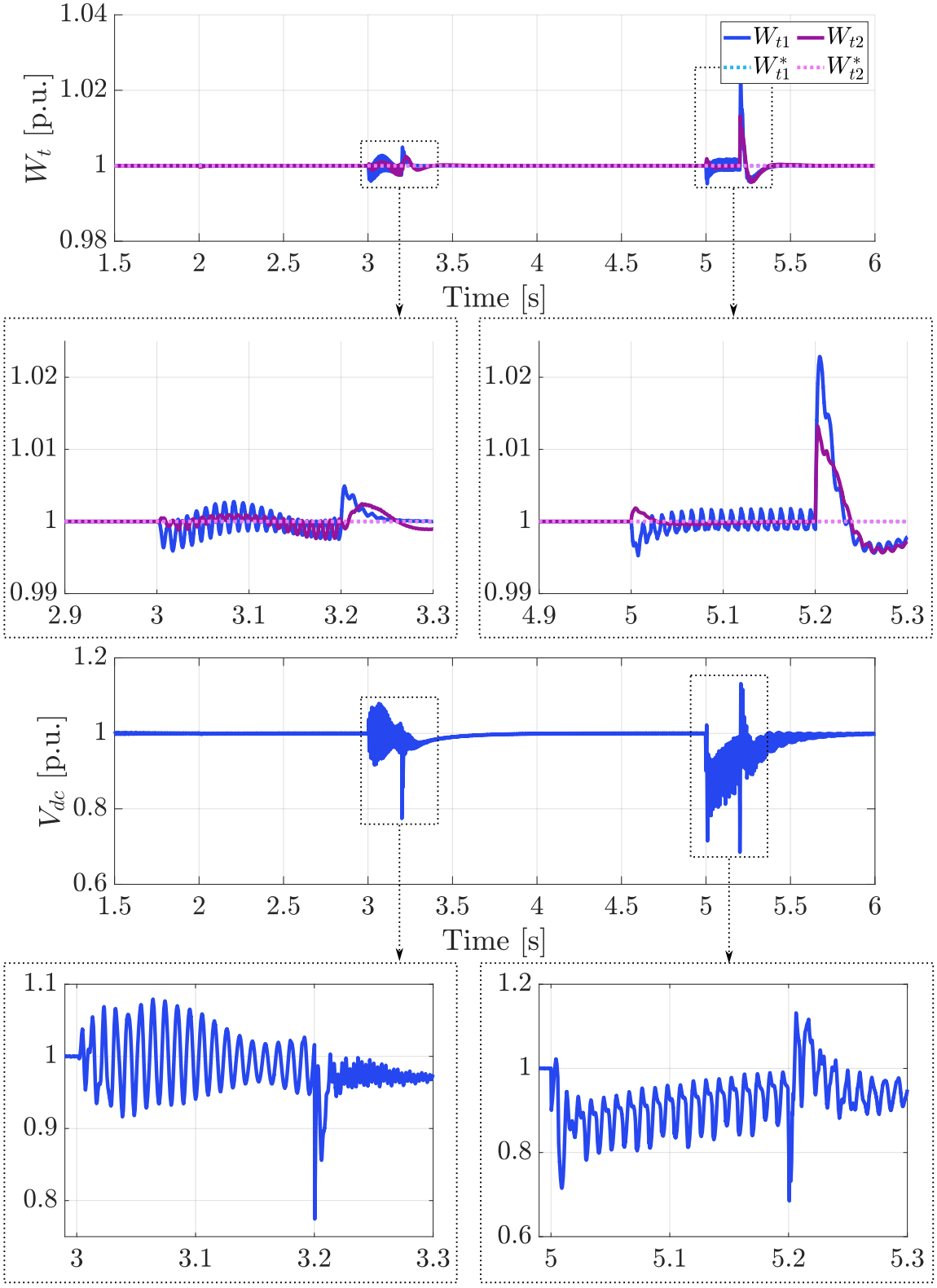


Figure 25: DC voltage and total energy in classical control.

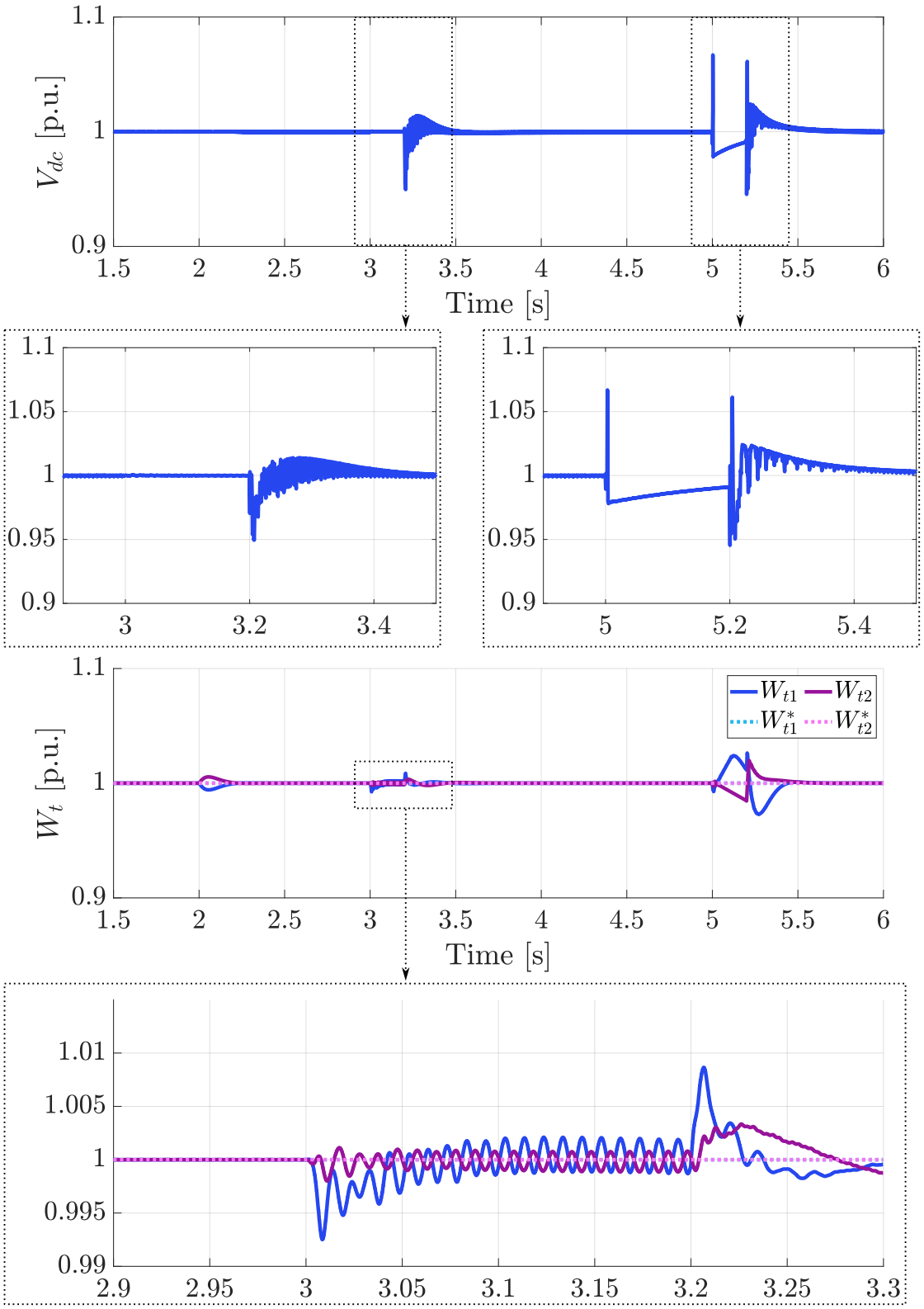


Figure 26: DC voltage and total energy results with crossed control.

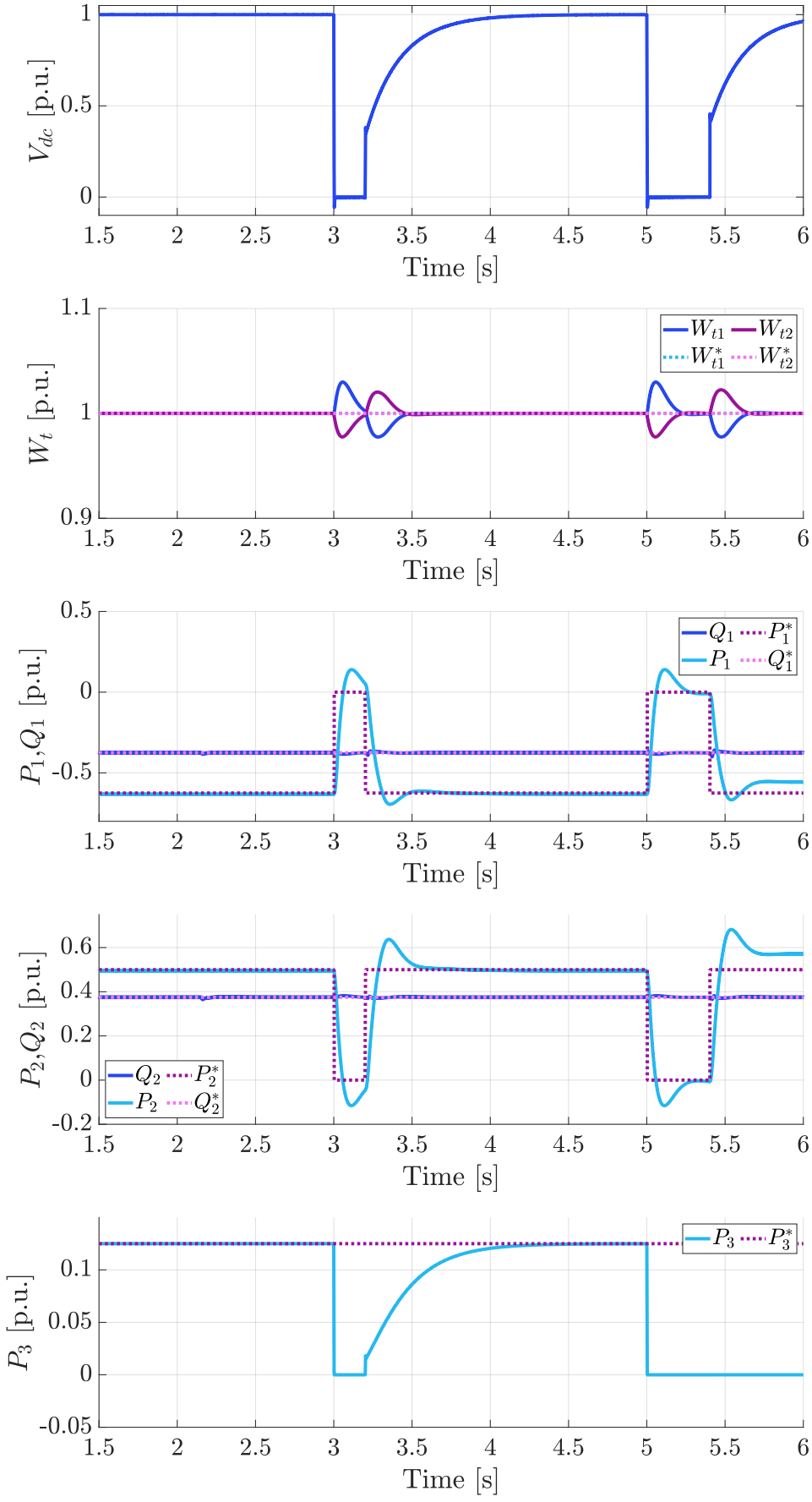


Figure 27: DC voltage and total energy results with crossed control and DC faults.

With the DC fault, as the DC bus is not available, no active power could pass between ports. However, the ports manage to at least still provide reactive power, allowing them to operate as STATCOMs, when DC faults occur.

5.2.3 Scenario 3: Combined Control

Based on the results obtained in the previous sections, it can be concluded that, when an AC fault occurs near a terminal, classical control ensures the regulation of total energy, while crossed control guarantees DC voltage regulation. Therefore, an interesting scenario would involve port 1 operating under crossed control, while port 2 operates under classical control. In this setup, the port with more available active power would focus on maintaining DC voltage, while the port unable to exchange power would prioritize stabilizing its total energy.

The results obtained from this specific case are shown in Fig. 28.

In this case, similar conclusions from Scenario 1 and 2 can be obtained regarding the balancing of the submodules. However, during balanced faults, the total energy of both ports remains controlled. Furthermore, the DC voltage is well-regulated, with smaller variations compared to the classical control case. During balanced faults, the DC current adjusts to maintain DC voltage stability and regulate total energy.

These results demonstrate that the combined control strategy effectively manages both balanced and unbalanced AC faults. However, this strategy requires a more complex configuration in the MPC, as both ports must implement both control strategies. Additionally, an effective methodology must be developed to determine which control strategy should be applied in each specific case.

5.3 Control Hardware in the Loop Validation

This section develops a Control Hardware-in-the-Loop (CHIL) validation. CHIL tests are based in connecting a microcontroller to a HIL device. By doing that, a more real test of the control can be done, without the need of having a real system representing the MMCs, which is economically not feasible. To implement the CHIL test a Texas Instrument F28379D microcontroller is used with the HIL TI LaunchPad Interface. The TI C2000 package included in Typhoon HIL's Marketplace [30] is also used for automatically generating control code that can be deployed directly to the microcontroller. Inside the microcontroller is implemented the centralized control, while the MMC controls and the grid are maintained inside the HIL device. It has been decided to maintain the MMC control inside the HIL due to analog inputs limitations of the microcontroller. In addition, the active power references obtained from the microcontroller are send to the HIL device as digital signals by using a

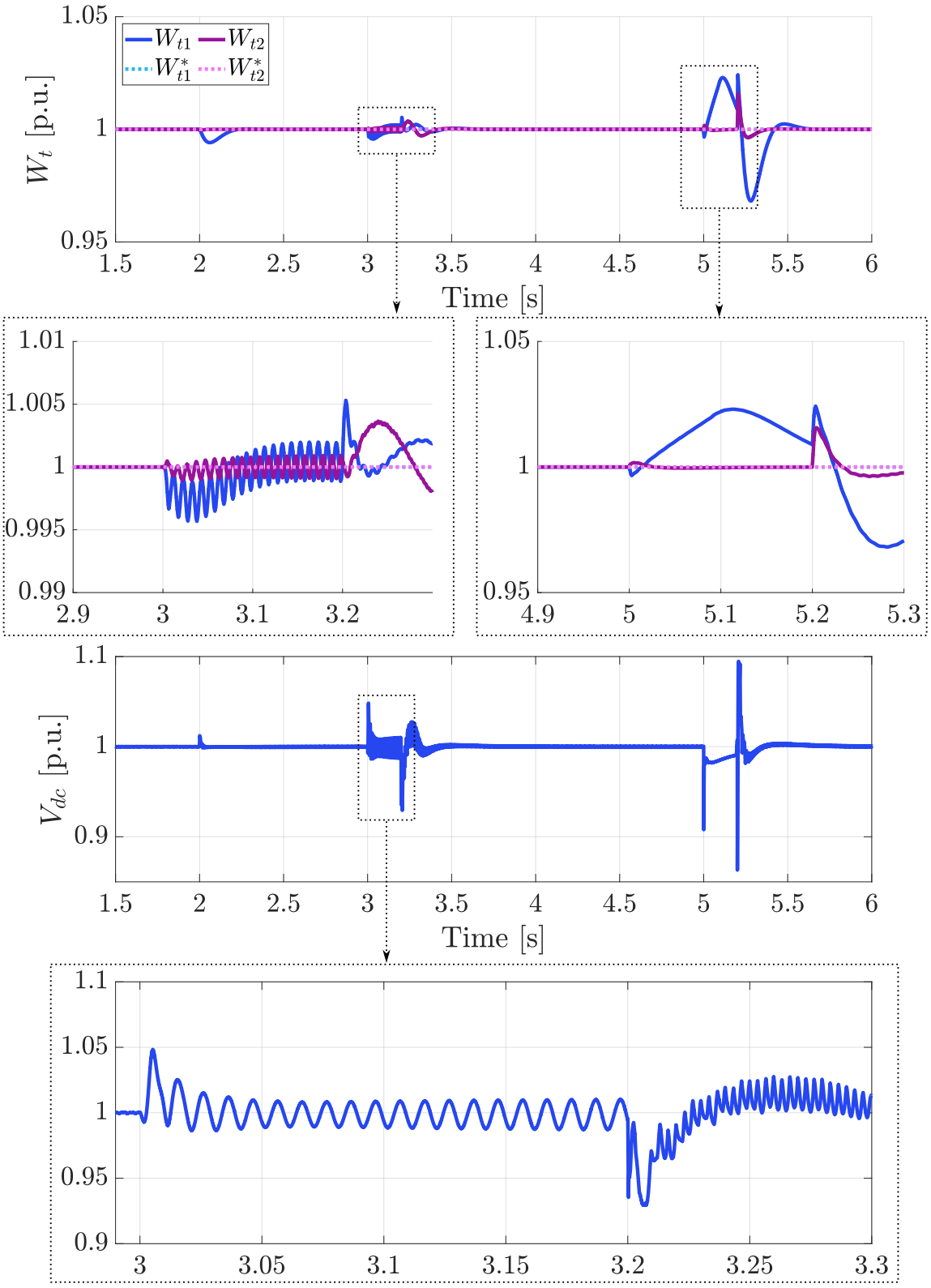


Figure 28: DC voltage and total energy with combined control.

PWM at high frequency. Then, on the HIL side they are converted again to analog signals by using the PWM Analyzer block available in Typhoon. Consequently, HIL606 firmware configuration 1 is used in order to support the use of PWM Analyzers. Fig. 29 and 30 show the setup of the validation test.

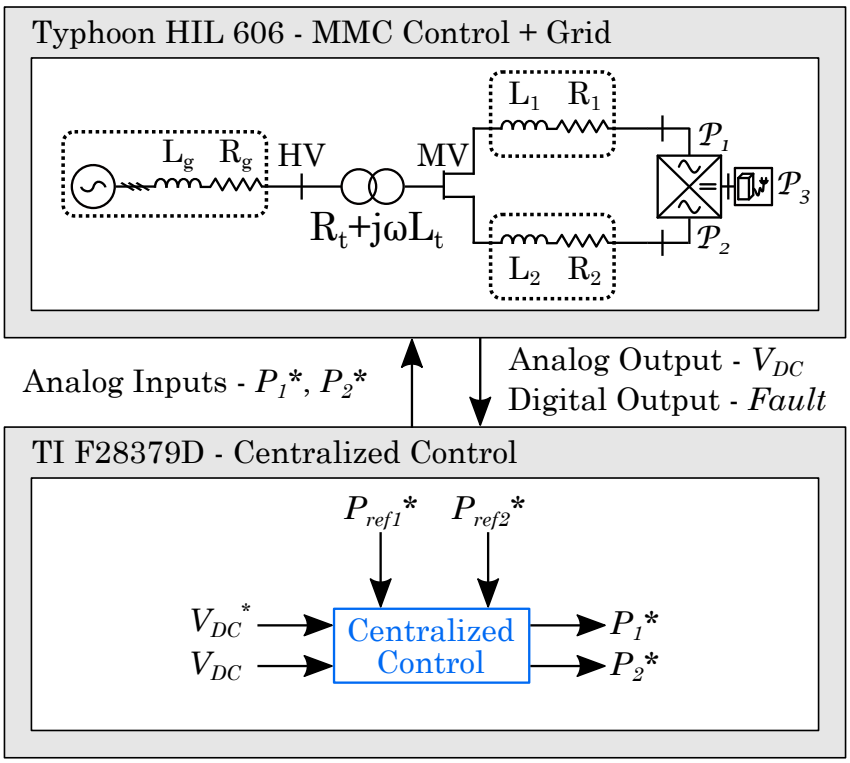


Figure 29: Schematic of the CHIL setup.

As the firmware configuration 1 is used, the maximum number of PWMs modulators is 12. So, one MMC is modelled in switching mode with 2 HB-SMs per arm, while the other operates as an averaged model to ensure that the cores could simulate the model in real-time. Should be mentioned, that with parallelization of HIL devices, both ports can be defined as switching MMCs. Fig. 30 illustrates in more detail the modelling and control inside the Typhoon HIL device.

To validate the control, a balanced fault near P_2 is done. In addition, the parameters of the simulation are changed to adapt at the new topology, with 2 SMs per arm. The new values are defined in Table III.

5.3.1 Combined Control

As demonstrated in Section V, the combined control strategy obtained the best results with AC faults. Consequently, this structure is validated with CHIL. In this case, to demonstrate that the MPC control is correctly designed, all the significant variables are shown in Fig. 31. The performed test is a deep balanced fault between 0.5 s and 2.5 s close to port 2.

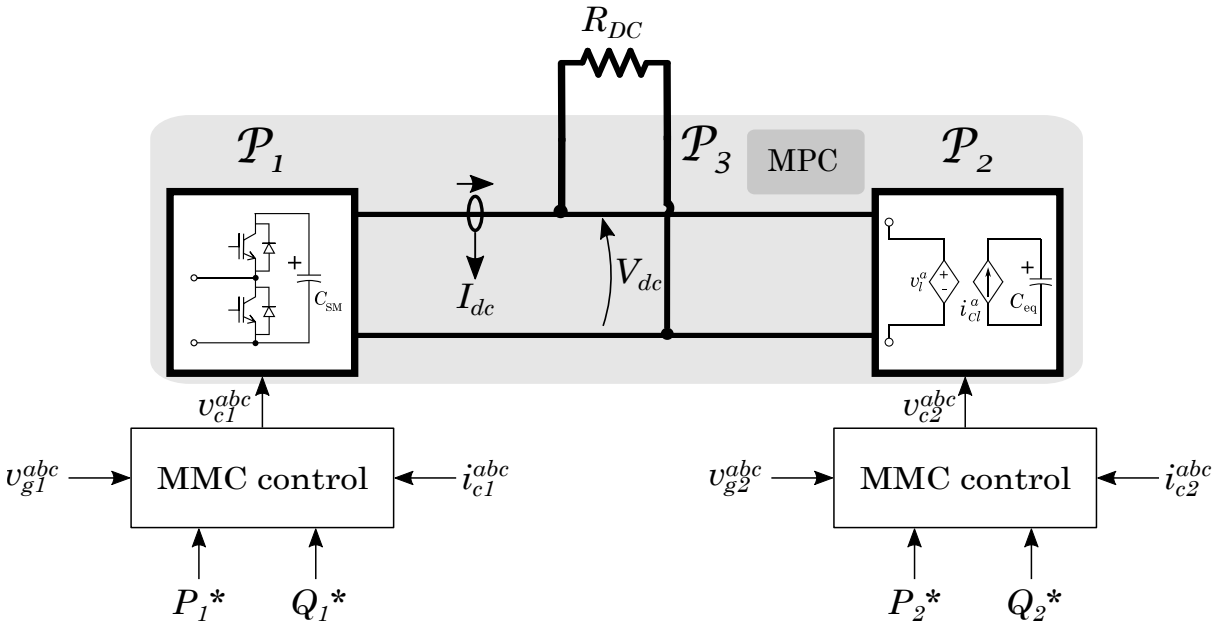


Figure 30: Modelling and control inside Typhoon HIL device with CHIL validation.

Table 7: CHIL validation parameters

Parameter	**Value**
Controller sampling time, T_s	0.1 ms
Typhoon sampling time, T_e	50 μs
Nominal AC grid voltage, V_{ac-N}	2.2 kV
Nominal port power, S_{c-N}	800 kVA
Nominal DC bus voltage of MPC, V_{dc-N}	4 kV
Short Circuit Ratio, SCR	10
R/X Ratio, R/X	1
Number of SMs per arm, N_{arm}	2
Sub-module capacitance, C_{SM}	10 mF
DC filter, C_{DC}	1.69 μF
Modulation frequency, F_s	10 kHz
AC port active power references, P_1^*, P_2^*	-0.625 p.u., 0.5 p.u.
AC port reactive power references, Q_1^*, Q_2^*	0.375 p.u., -0.375 p.u.
DC voltage reference, V_{dc}^*	1 p.u.
DC Load active power reference, P_3^*	0.125 p.u.
Grid impedance, R_g, L_g	0.7R_{eq}, 0.7L_{eq}
Feeder 1 impedance, R_1, L_1	0.3R_{eq}, 0.3L_{eq}
Feeder 2 impedance, R_2, L_2	0.3R_{eq}, 0.3L_{eq}
Coupling impedance, R_l, L_l	0.01 p.u., 0.2 p.u.
Arm impedance, R_a, L_a	0.01 p.u., 0.2 p.u.

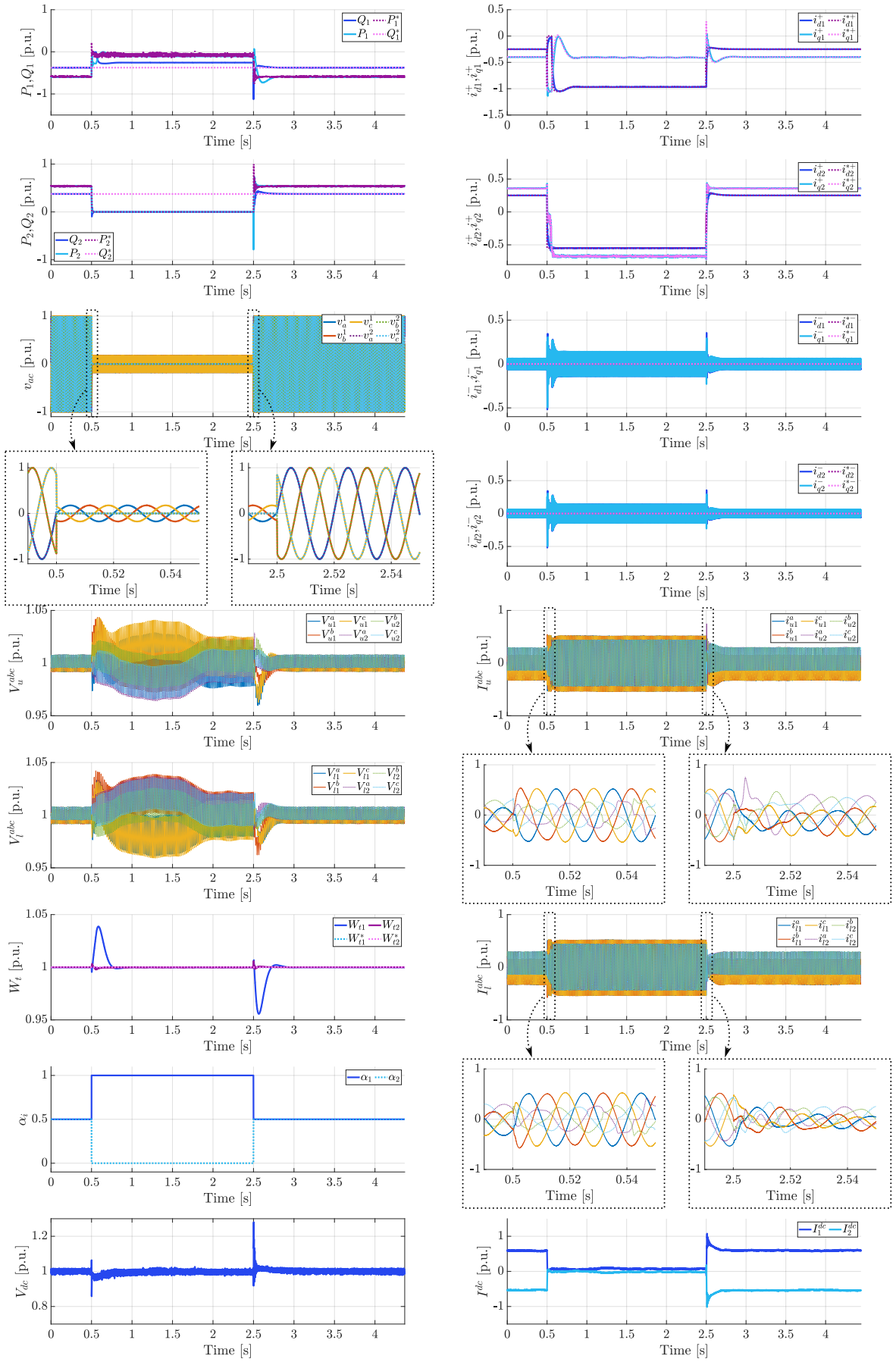


Figure 31: CHIL validation with combined control.

The obtained results demonstrate the validity of the proposed controller for the MV MPC. In addition, it should be noted that during the deep fault the voltages of the MPC are not balanced between them, as a consequence of the disconnection of the AC additive current control.

5.4 Conclusion

In this section, a comparative analysis of control strategies for a non-isolated MV-MPC based on a FB-MMC topology has been made. Both classical and crossed control approaches are investigated and compared, assessing their performance in normal and abnormal conditions. It is shown that a combined strategy leverages the strengths of both approaches, improving the MPC's robustness and this strategy is validated both through simulations and in a CHIL setup.

6 Experimental validation of the selected MPC topology

In this chapter, a small-scale and modified version of the selected multi-port converter topology will developed and its performance will be verified in the lab.

6.1 Description of the lab prototype

Based on the evaluation and ranking in the previous chapter, the topology in Fig. 32 is chosen. It consists of two MV AC-ports (port 1, V_{1abc} and port 2, V_{2abc}) realized by modular multilevel converters using FB-based sub-modules. The FB SMs are important to realize AC-voltage levels independently of the comment DC-link voltage which is important characteristics for interconnecting different AC voltage levels. The intermediate DC voltage is then reduced to a low voltage DC port (port 3, V_{DC}) through an isolation by high-frequency DC-DC conversion stage as described in the previous chapter. The input-series and output-parallel configuration of the isolation stage is to handle the medium-voltage input side and high-current output side of the DC-port.

The selected topology is intended for a voltage level of 5/20/40 kV on the AC-ports and 400 V on the DC-port. With a MV on the AC-ports and a DC-voltage level of similar magnitude in the interconnection, an isolation stage to scale down this voltage level to 400 V is necessary. However, all the voltages in the lab prototype are low ($V_{1LL,rms} = 50\ V$, $V_{2LL,rms} = 100\ V$, and $V_{DC} = V_3 = 100\ V$) and hence the isolation stage which uses input-series output-parallel connected DAB DC-DC converter stages to reduce the common DC-link voltage to low-voltage DC-port voltage is skipped. Of course, for a test with higher voltages and available resources, the actual setup can be realized. Due to this, the DC-port is realized in the lab with a non-isolated direct connection to the DC-link with the DC-voltage of the interconnection directly controlled to the DC-port voltage needed. The two voltage levels on port 1 and 2 are realized using a two-level converter (Fig. 33-a) and a multilevel converter using FB cells (Fig. 33-b) [52], respectively. There are 4 SMs, whose capacitor has capacitance of 0.5 mF and an ESR of 50 mΩ, per arm for each phase and their capacitor voltage is nominally set to 50 V. Each arm of the MMC has a series resistive-inductive filter of 2.3 mH and 60 mΩ. In addition, port 2 is connected to an AC-grid realized through a grid-emulator (Fig. 33-c) [53] where as port 1 is connected to a passive load. The DC-port is connected to a resistive load or a DC-voltage source (Fig. 33-d) which acts as the energy storage. Using the lab components, the block diagram of the complete laboratory setup is shown in Fig. 34.

6.2 Main controllers of the lab prototype

The main controllers at the three port terminals is described briefly in this section.

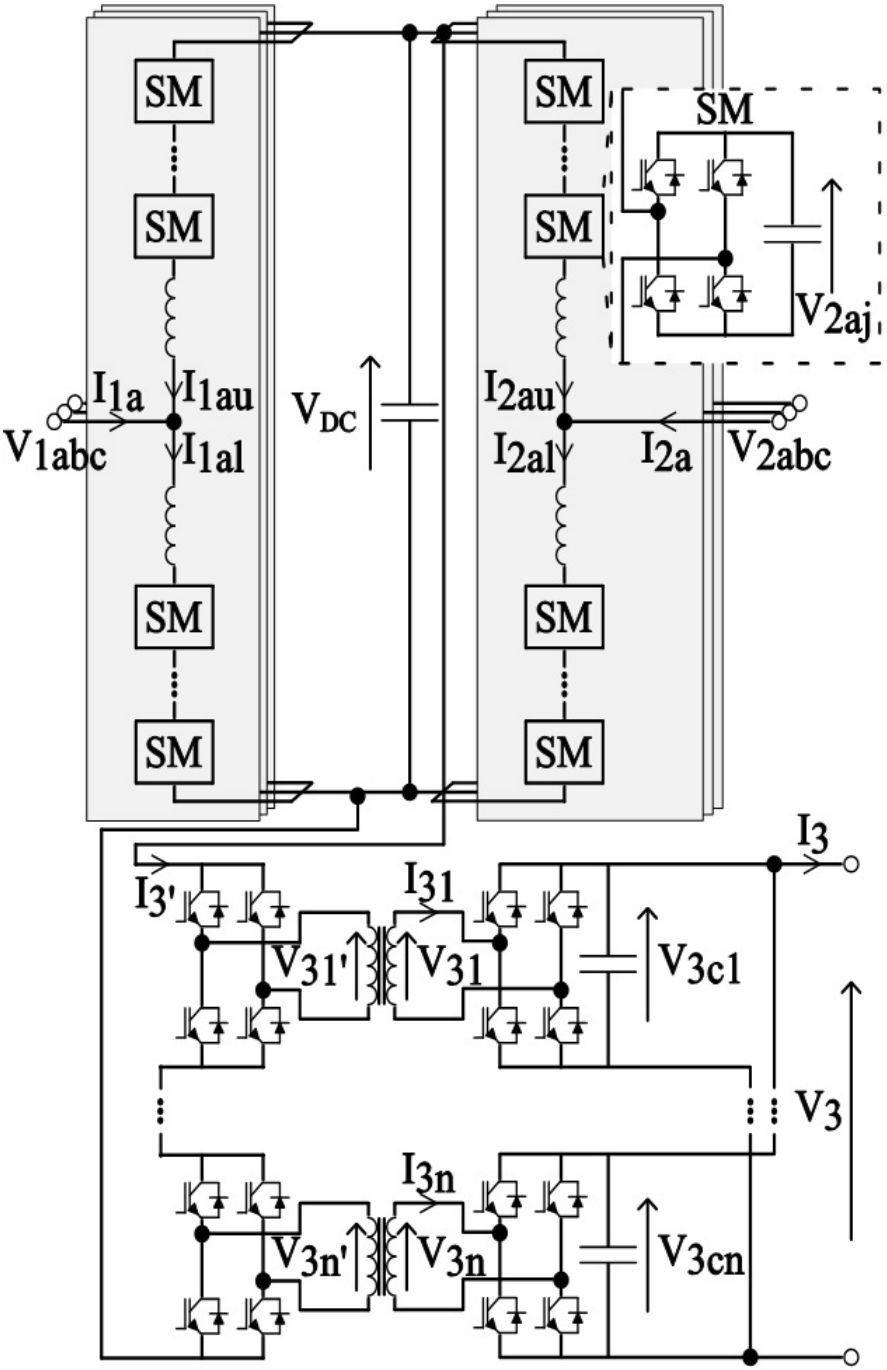


Figure 32: Schematic of the selected semi-isolated topology

6.2.1 Multilevel converter - AC port 2

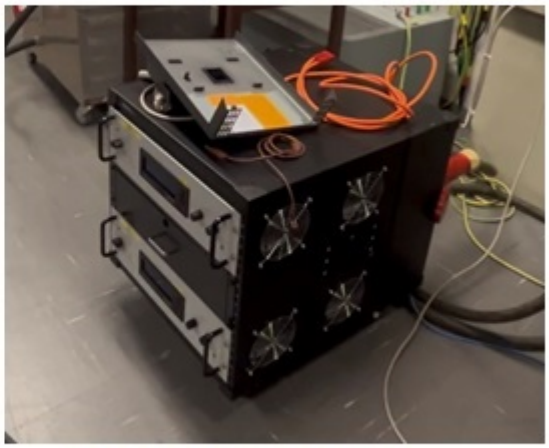
The three-phase MMC is controlled using the classical approach of grid-following control on the AC-side in a synchronous dq-reference frame, where the various control loops that are implemented to run the lab setup will be described briefly here.

Phase-locked loop (PLL): This loop will generate the grid voltage angle such that the d-axis of the synchronous reference-frame aligns with the dq-voltage vector of the PCC.

(a) Two-level converter

(b) Multilevel converter

(c) Grid emulator



(d) dc voltage source

Figure 33: Components to make up the lab prototype.

As such, d- and q-components of the current vector represent active- and reactive-power generating components for the control loops. For this loop, a proportional-integral (PI)

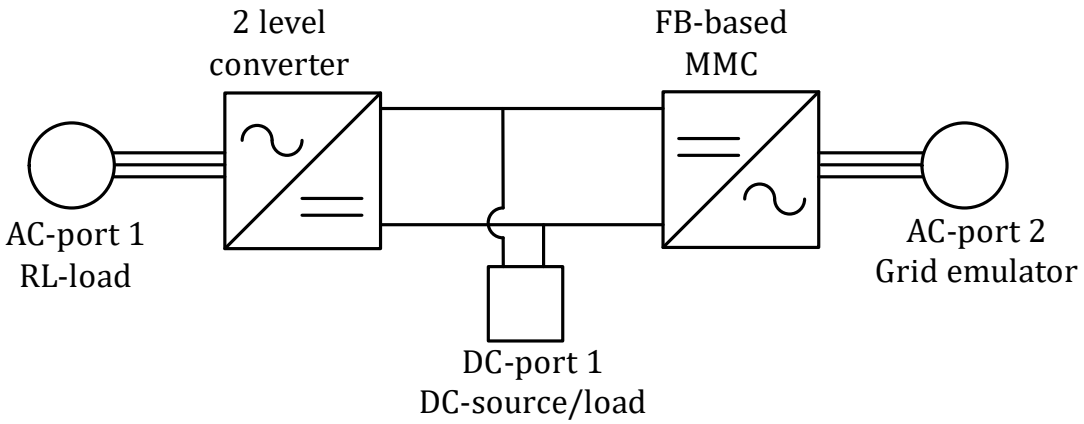


Figure 34: Block diagram of the laboratory setup.

controller is used to track the grid frequency and an extra integrator to generate the angle. The loop bandwidth is adjusted by tuning the proportional-integral (PI) gains [51].

Reactive-power controller: This control loop generates the reference reactive-current to have a closed-loop control of the reactive power.

Energy controller: This control loop generates the reference active current to control the sum of all capacitor voltages to a reference value. For this, a classical PI-controller is chosen. With the active power output at port 1 and 2 controlled at their respective loads, the active power that is transferred to port 1 is automatically set through the energy controller. To improve the dynamic performance, a feed-forward term can be added to the generated reference active-current corresponding to the steady-state active power transfer to AC-port 1.

DC-link voltage controller: As the DC-link voltage and the total SM capacitor voltages using FB cells is unrelated, we need another degree of freedom to control the DC-link voltage. One option is to use the other ports to provide DC-link voltage control and that requires a controlled active-power exchange. However, when only loads are connected on these terminals, the DC-link voltage control is provided by using PI-based DC-link voltage controller where the output of which generates the DC-component of the circulating current for all the three legs of the converter. An optional smoothing buffer capacitor can also be used to attenuate high-frequency voltage ripples from the PWM modulation.

Energy balancing controller: Similar to the DC-link voltage controller, the sum SM-capacitor voltage of each-phase leg is controlled to a reference value by generating an additional DC-component of the circulating current for each phase which will be added to the outputs of the DC-link voltage controller.

AC-side current controller: This loop generates the reference converter voltage with a closed-loop current control where the reference-currents are obtained from the outer loops. A PI-based controller with a grid-voltage feed-forward and a current cross-coupling

compensation is implemented [51]. From the reference voltage and the sum of capacitor voltages in each phase, the modulation index for each phase is generated. To counteract the impact of unbalanced voltages, a negative-sequence controller is also included.

Circulating current controller: In order to attenuate the 100 Hz circulating current within the legs of the MMC, a PI-based circulating current controller is implemented. The DC-component of the circulating current is controlled to a value decided by the DC-link and energy balancing controllers, and in steady-state fulfills the active power balance from all the ports.

Modulation: With the number of SMs in the arm being low at 4, pulse-width-modulation (PWM) with a carrier frequency of 20 kHz is used to bypass or insert the FB sub-modules with positive or negative capacitor voltage to generate the converter-voltage output. The keep the SM capacitor voltages balanced, sorting is also implemented the modulation scheme.

6.2.2 Two-level converter - AC port 1

With DC-side of the converter controlled from the MMC converter side, AC side is operated with nominal voltage to supply a passive load. If an AC-grid is connected to this converter, the control on the AC-sde can be adopted similar to the MMC converter. In this case the control of the DC-link voltage can have various alternatives.

6.2.3 DC-port load/source

The DC-port voltage has to be controlled in order to support connecting an energy storage, PV, or DC-load at this terminal. With a direct connection to the DC-link voltage, only a load or source absorbing or injecting a certain active power is connected. This power exchange with the DC-link should be managed with other AC-terminals to have the power balance. As the interesting dynamics are on the MMC side, measurements related to that converter are plotted.

6.3 Operation of the multiport converter

With the selected prototype as described previously, operation in normal conditions during active- and reactive-power changes and abnormal conditions during voltage dips (balanced and unbalanced) and port disconnections are tested on the setup. With AC port 1 connected to an RL passive load and the output of the two-level converter voltage output set to 50 V and the DC-port is connected to a resistive load, the wave-forms from the MMC both on the DC-side and AC-side (AC-port 2) are presented to show the dynamic performance of the multiport converter. Steps in the active-power output are made by changing the load

connected to the DC-port or the AC-port 2. To plot the results in per-unit (pu), base values of voltage (3-phase, line-to-line, RMS) of 100 V, apparent power of 1000 VA, and the corresponding current-base are used. In addition, a DC-voltage base of 100 V and a DC-current base of 10 A is used to plot DC-related signals such as SM capacitor voltages, DC-link voltages, DC-side current and circulating current.

6.3.1 Dynamic performance in normal conditions

The results in this section shows operation of the converter in normal conditions (active and reactive power steps at different ports) with the setup as described previously. The first set of results in Figs. 35 - 38 shows that the MPC operates as expected with a reactive-power step at AC-port 2 and all the quantities are controlled to the desired values. The active-power on AC-port 2 as shown in Fig. 36 changes to account for the losses due to the increase in reactive power where as the power on the DC-side of the MMC is unchanged as seen from the waveforms of the DC-link voltage and DC-side current in Fig. 37. The total energy and individual SM capacitor voltages are also controlled within the required limits as shown in Fig. 38.

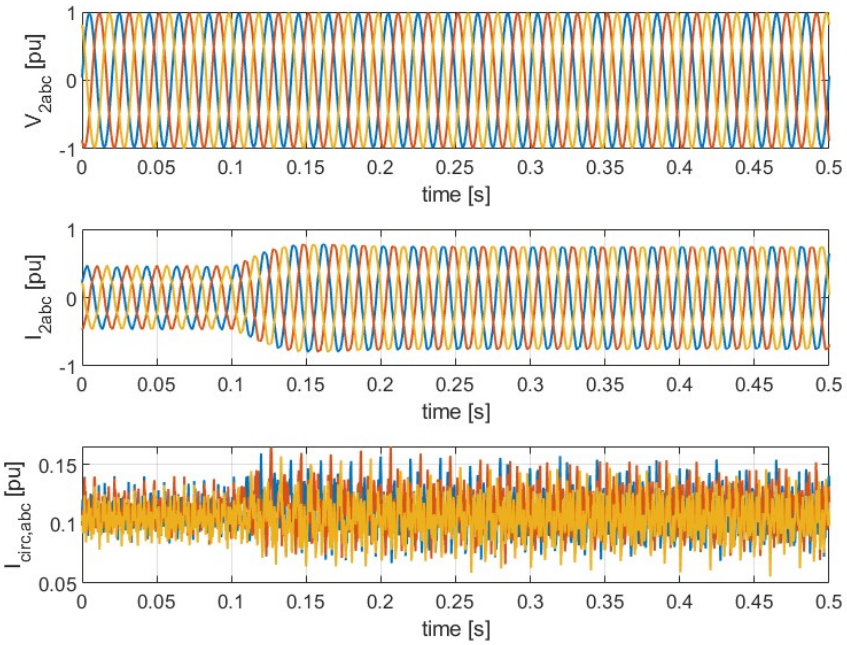


Figure 35: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); a reactive-power step-up happens at 0.1 s at port 2.

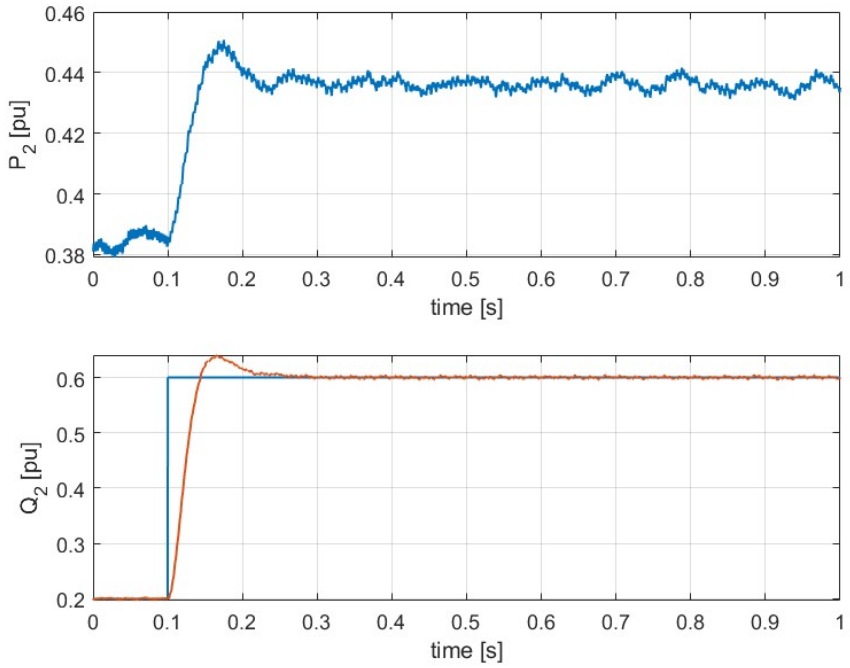


Figure 36: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); A reactive-power step-up happens at 0.1 s at port 2.

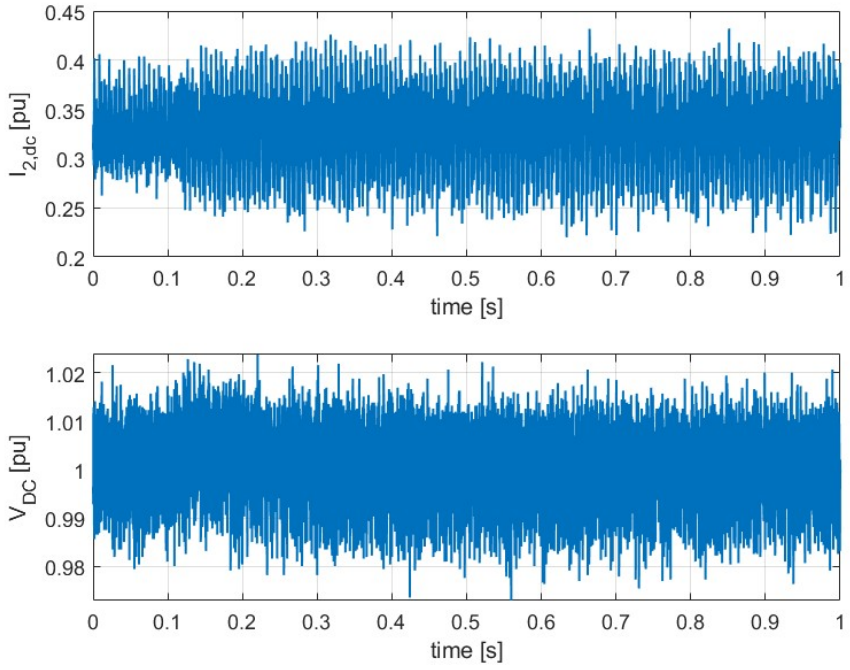


Figure 37: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; a reactive-power step-up happens at 0.1 s at port 2.

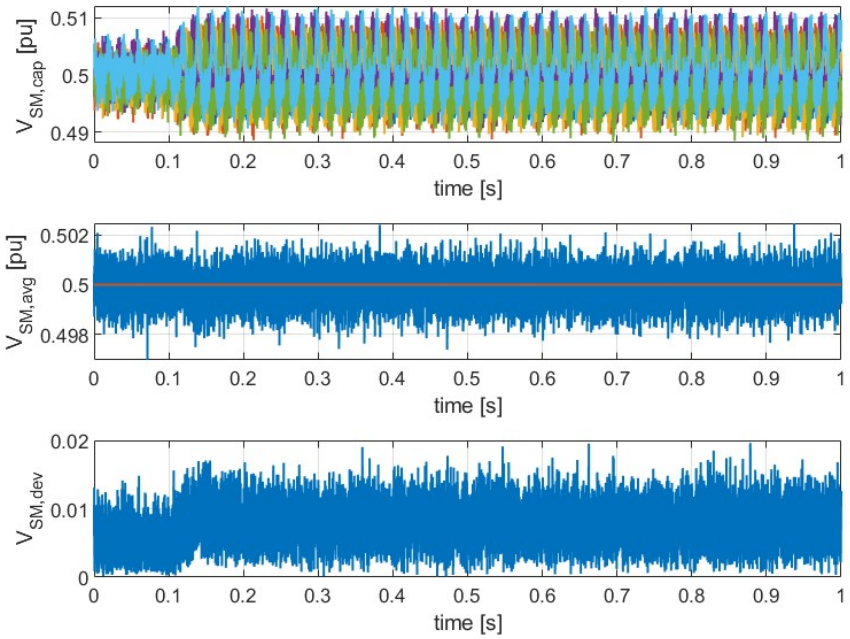


Figure 38: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; a reactive-power step-up happens at 0.1 s at port 2.

Next, changes in the active power at the DC-port (both stepup and stepdown) are applied to test the operation of the converter and results are presented in Figs. 39 - 46. As the results indicate all quantities are controlled within allowed limits with the active power output at AC port-2 as well as the SM capacitor voltages are regulated well. A change in active power also affects the DC-link but controlled to the reference value very well. The slow dynamics associated with the active-power output at AC-port 2 is due to the active-current component of the MMC regulating the SM capacitor voltages, which in general has slow dynamics due to the high capacitance it uses. Similarly changes in the active power at the AC-port 1 have been performed (both step-up and step-down) and the converter works as expected with power balance fulfilled. In the operation performed, the power flow is controlled with the capacitor voltage of all the sub-modules balanced and within limits. For varying power level in all parts, the DC-port voltage can be controlled close to the reference confirming a successful operation of the converter in normal conditions.

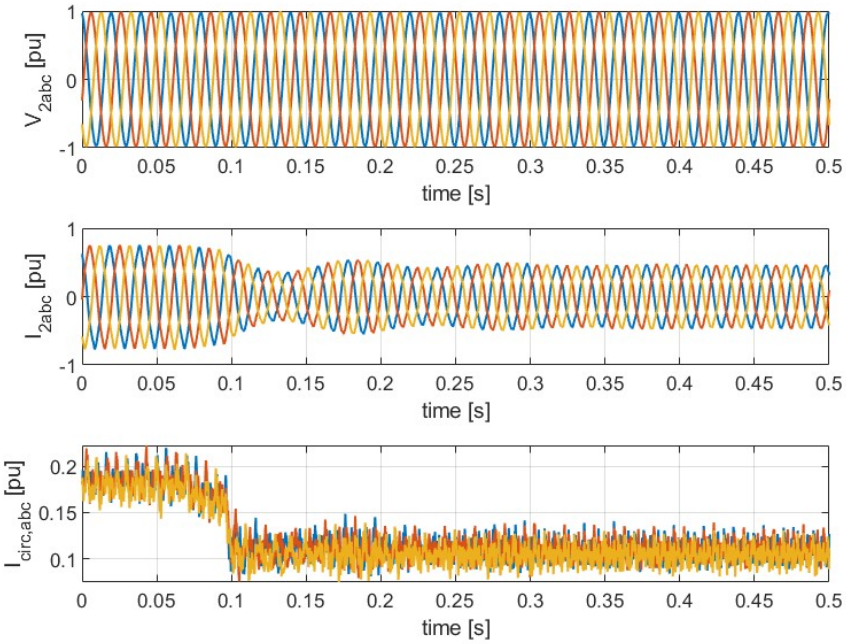


Figure 39: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); a load step-down happens around 0.1 s at the dc-port.

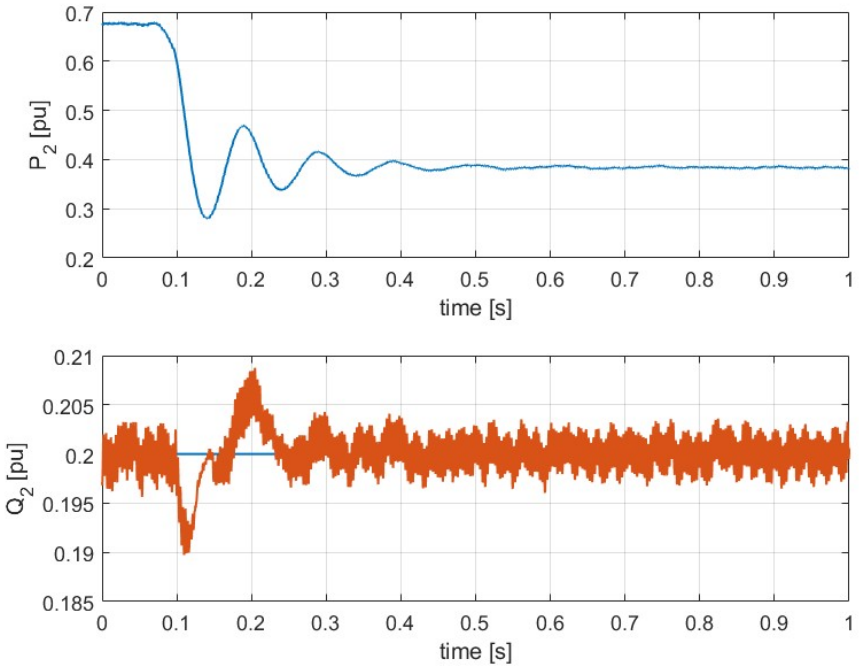


Figure 40: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); a load step-down happens around 0.1 s at the DC-port.

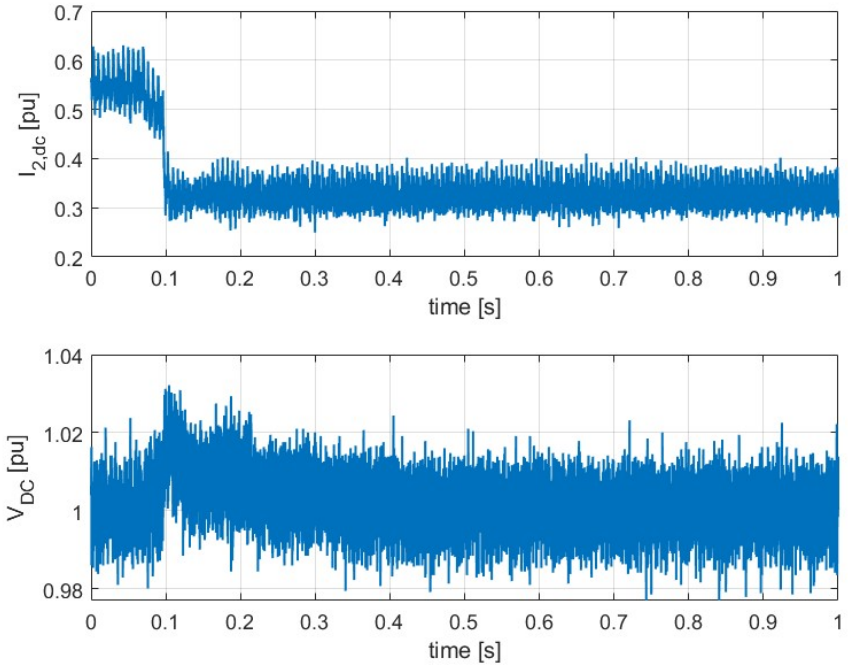


Figure 41: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; a load step-down happens around 0.1 s at the dc-port.

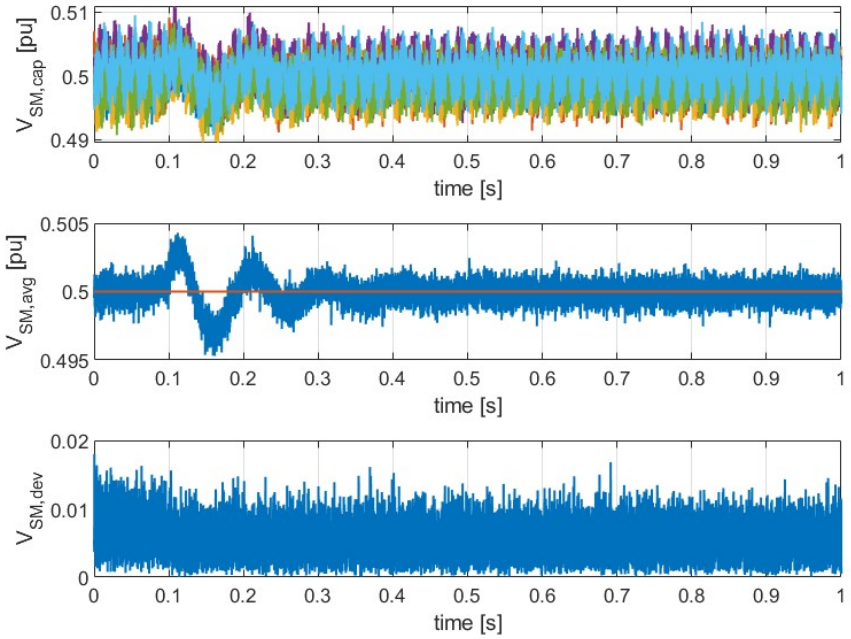


Figure 42: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; a load step-down happens around 0.1 s at the DC-port.

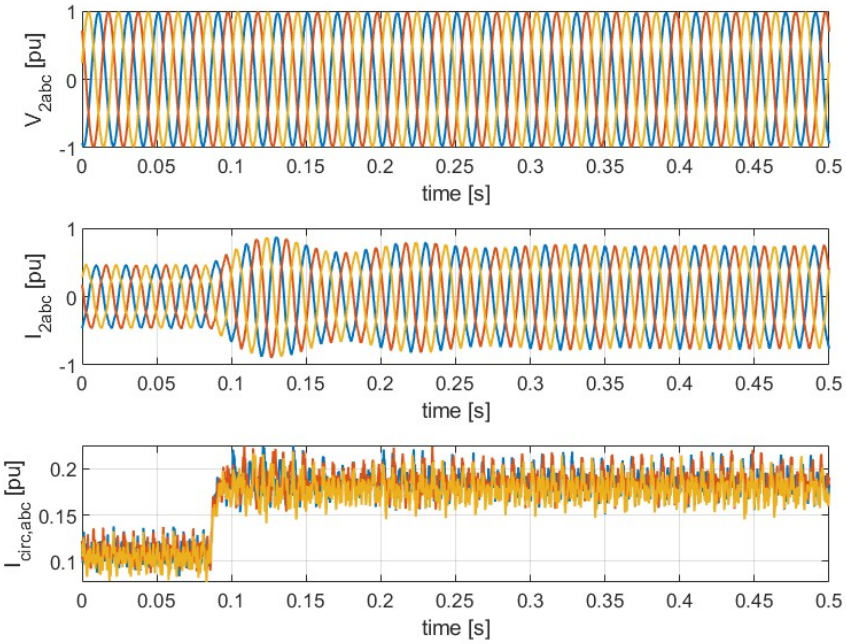


Figure 43: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); a load step-up happens around 0.1 s at the DC-port.

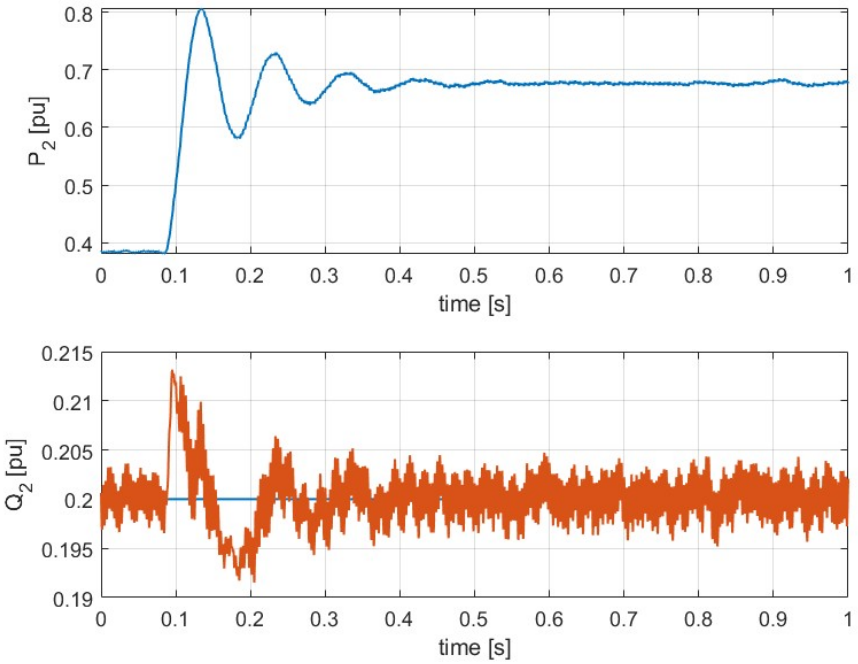


Figure 44: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); a load step-up happens around 0.1 s at the DC-port.

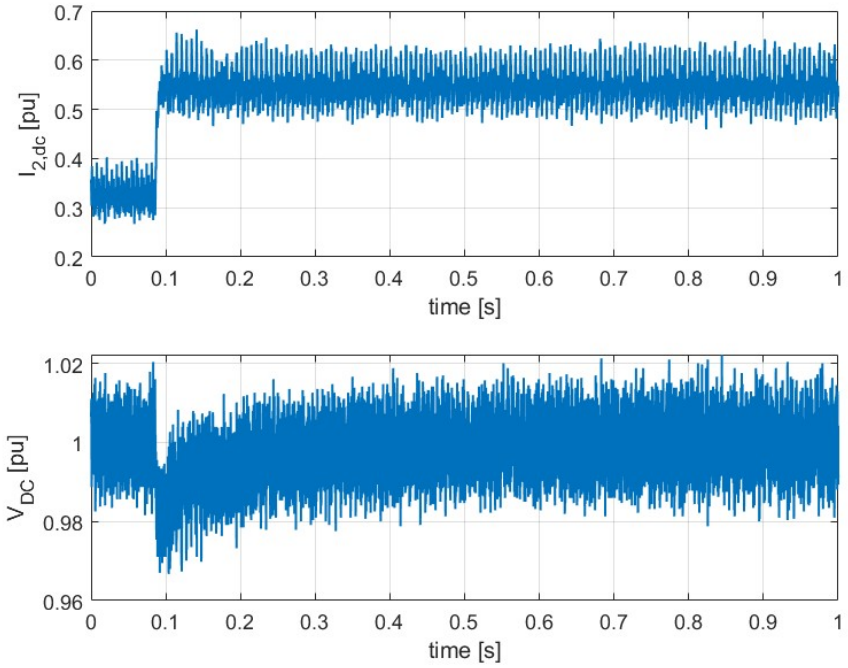


Figure 45: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; a load step-up happens around 0.1 s at the DC-port.

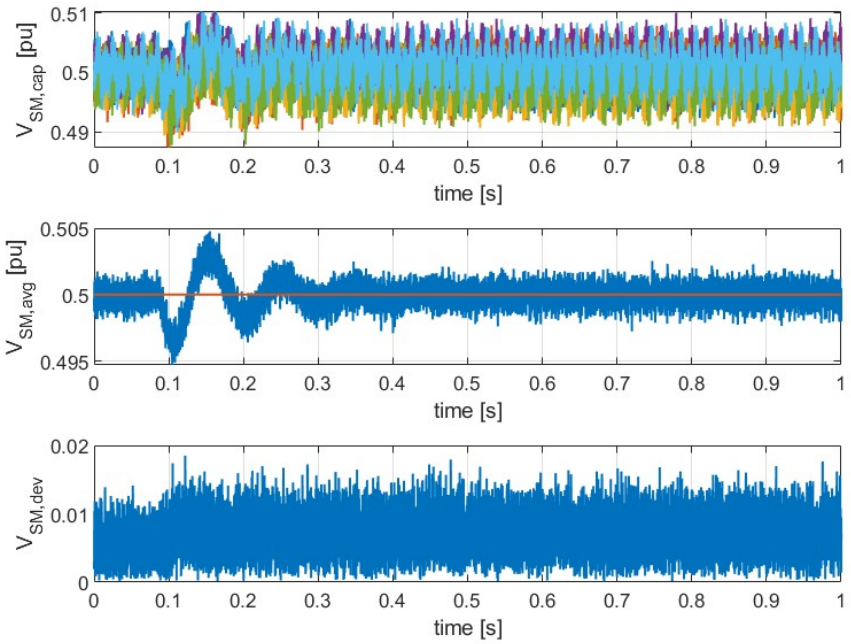


Figure 46: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; a load step-up happens around 0.1 s at the DC-port.

6.3.2 Impact of abnormal operation conditions

In this section abnormal conditions such as balanced voltage dips, unbalanced AC-grid operations, and a loss of one of the AC ports or the dc port, are demonstrated to evaluate the robustness of the MPC.

3-phase balanced voltage dip: When a symmetric three-phase voltage dip happens in the AC-grid as as in Fig. 47, depending on the ride-through strategy, the power exchange at the faulty port is managed through active management of the reference-active power and have a proper current limiting strategy. In this example, a voltage dip is applied to still be able to exchange demanded active- and reactive power and test the dynamic performance of the MPC during the voltage dip. The results in Figs. 47 - 50 show that the MPC operates well during the dip with a power exchange as required and the DC-port and SM capacitor voltages all within the controlled range. The slow dynamics displayed are initiated by an active- and reactive-power disturbance due to the dip that affects the SM capacitor voltage dynamics. The controller manages to achieve a stable operation of the converter. Similarly, the converter operation is tested when the dip is removed and results in Figs. 51 - 54 show that the converter successfully passes through the transient.

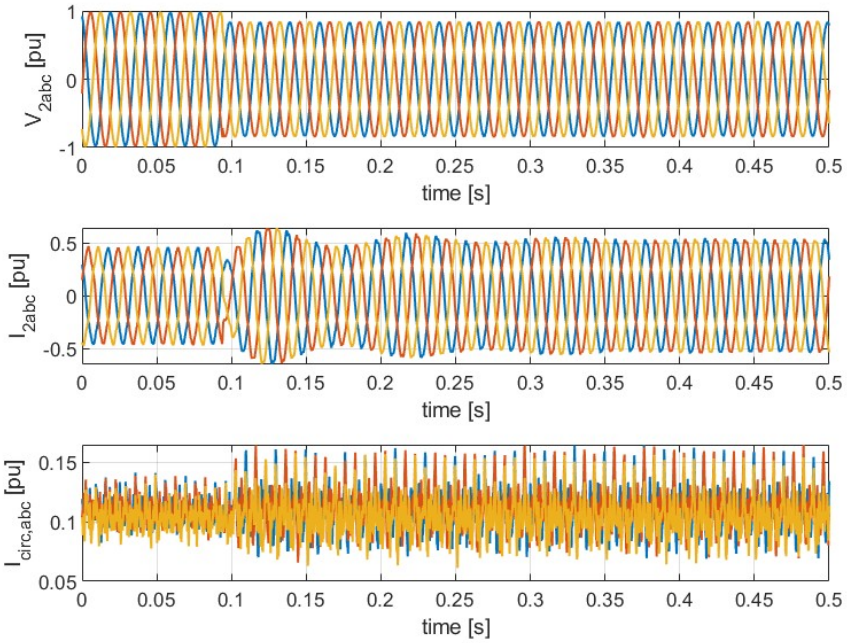


Figure 47: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); a three-phase balanced voltage dip happens around 0.1 s at AC-port 2.

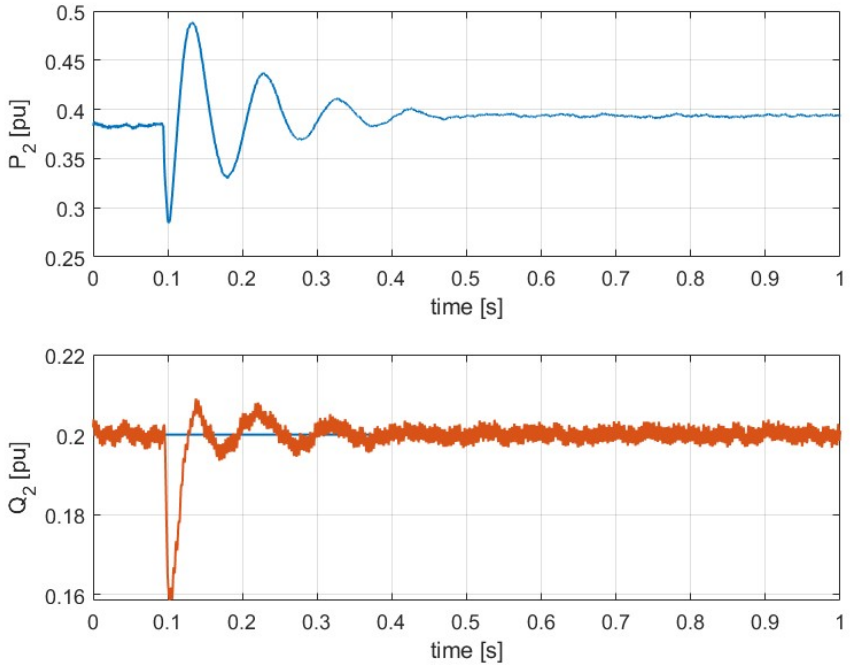


Figure 48: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); a three-phase balanced voltage dip happens around 0.1 s at AC-port 2.

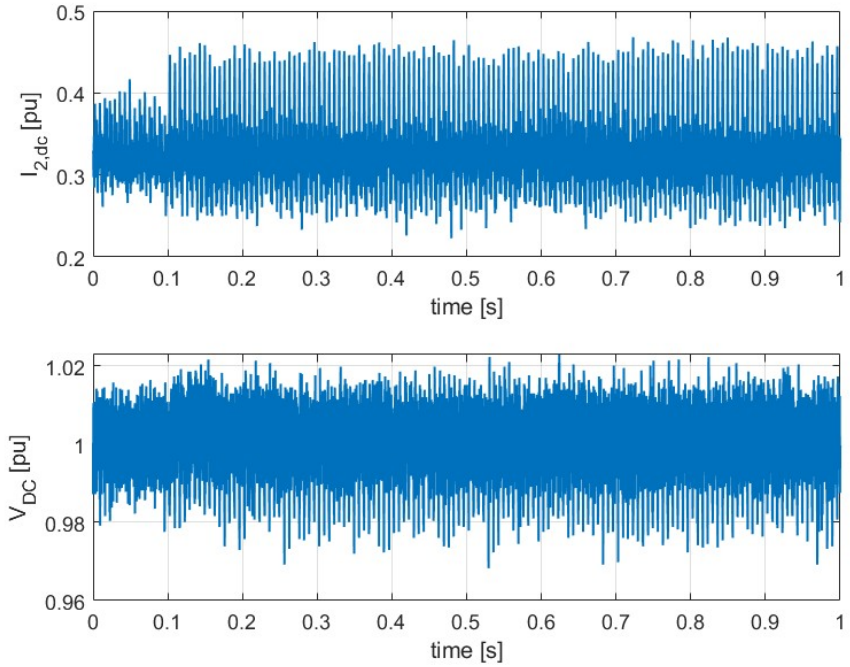


Figure 49: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; a three-phase balanced voltage dip happens around 0.1 s at AC-port 2.

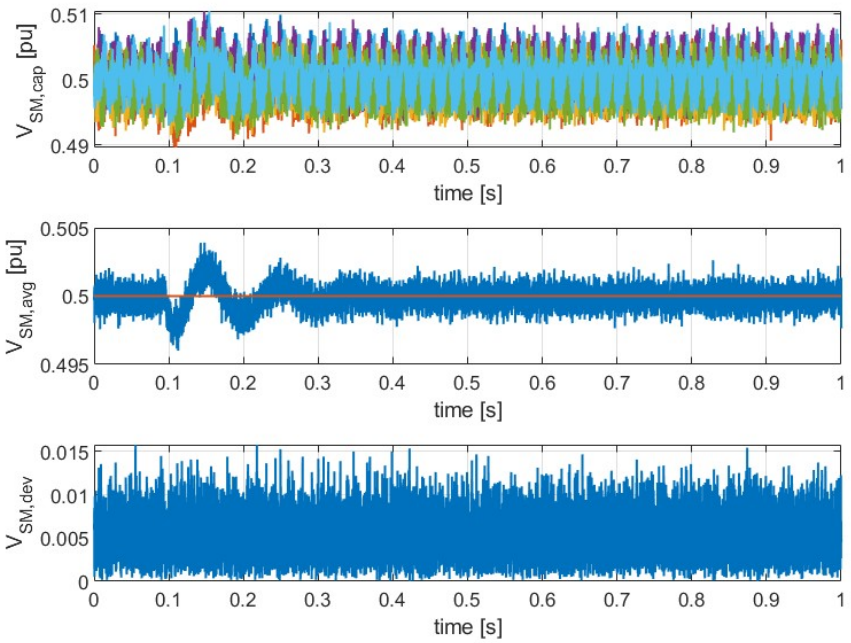


Figure 50: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; a three-phase balanced voltage dip happens around 0.1 s at AC-port 2.

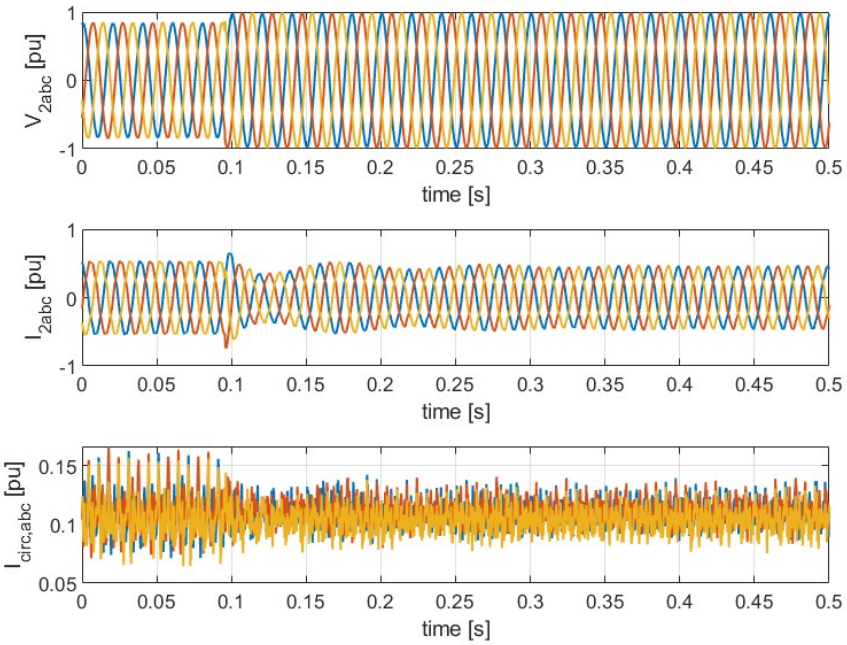


Figure 51: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); a three-phase balanced voltage dip is removed around 0.1 s at AC-port 2.

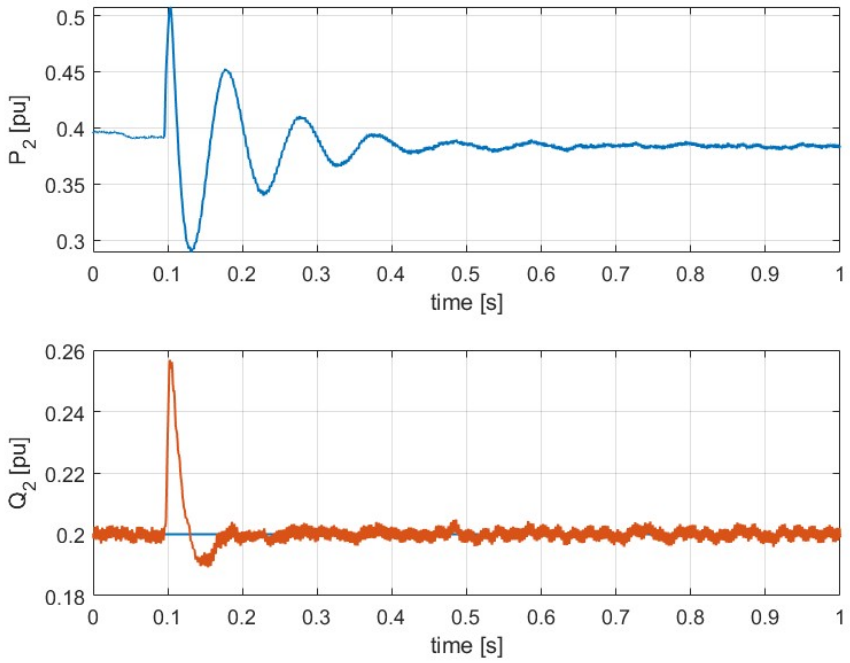


Figure 52: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); a three-phase balanced voltage dip is removed around 0.1 s at AC-port 2.

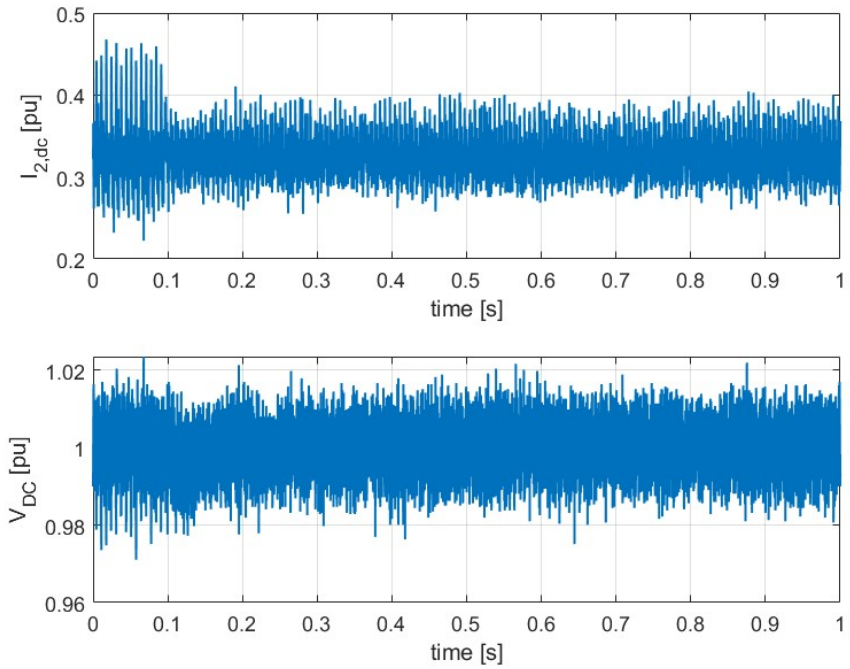


Figure 53: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; a three-phase balanced voltage dip is removed around 0.1 s at ac-port 2.

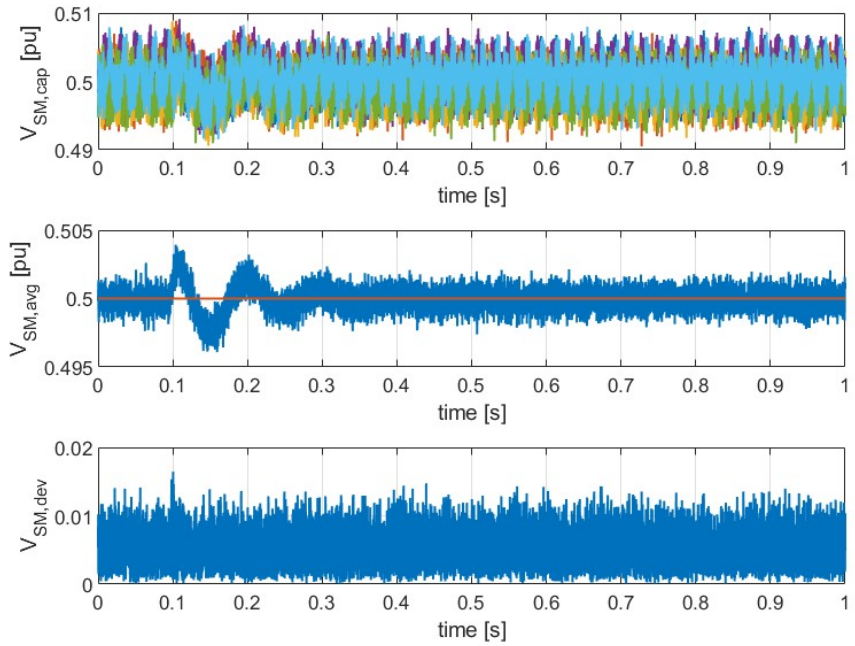


Figure 54: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; a three-phase balanced voltage dip is removed around 0.1 s at AC-port 2.

Loss of a port: Converter operation in normal conditions indicate that power on AC-port 1 and DC-port can be varied independently including sudden connection and disconnection of load on those ports. To show that the converter can operate in the loss of AC-port 1, the schematic in Fig. 32 is operated without the smoothing capacitor and the converter comprising of AC-port 1. With the same control structure for the MMC, a load change on the DC-port is made to see the operation of the converter. The results in Figs. 55- 62 show that the MPC functions well in time of loss of one of the ports. Similarly, the DC-port load can be totally disconnected (the load change in this case is to zero power consumption at the DC-port), in which case the MPC operates as a back-to-back converter.

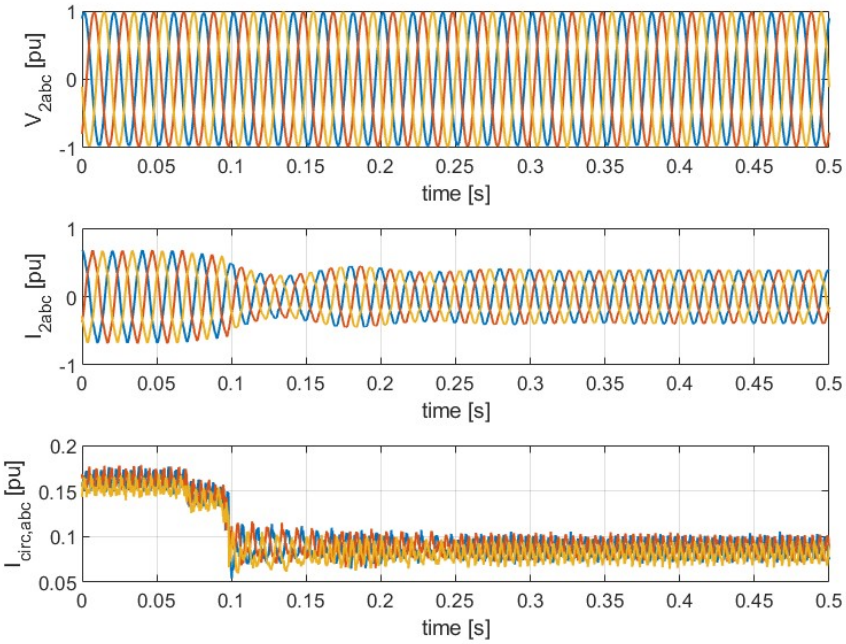


Figure 55: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); no AC-port 1 and a load step-down happens between 0.05 and 0.1 s at the DC-port.

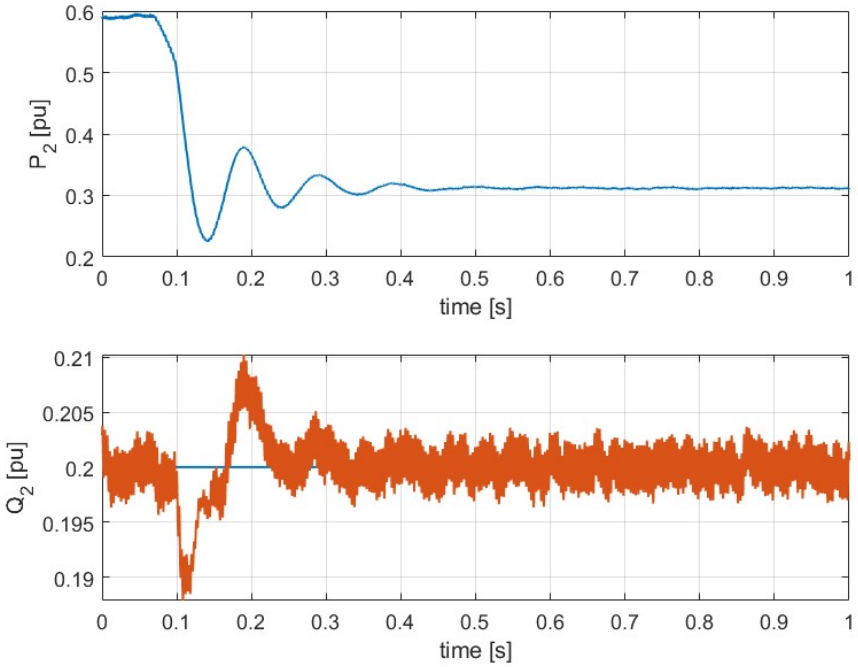


Figure 56: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); no AC-port 1 and a load step-down happens between 0.05 and 0.1 s at the DC-port..

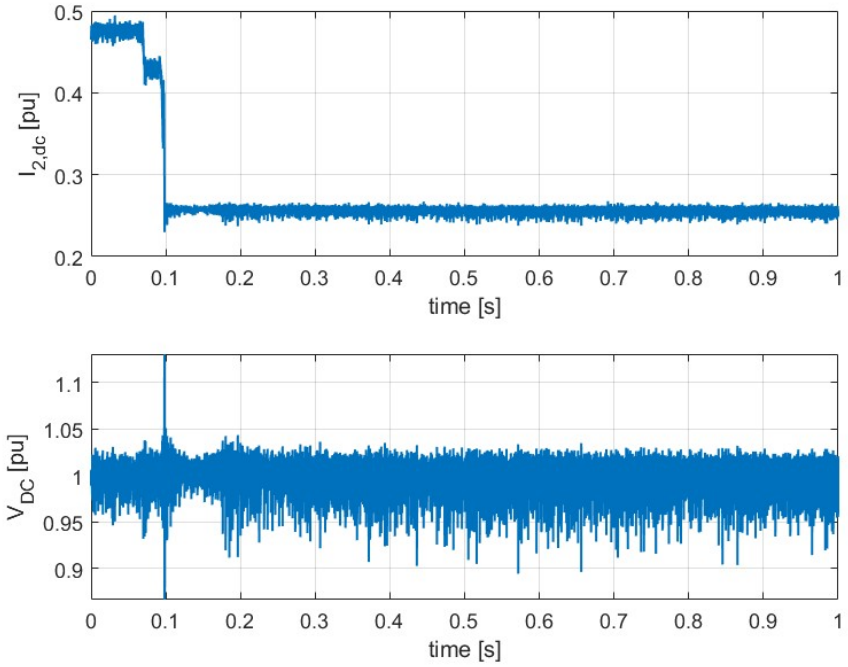


Figure 57: DC current from the MMC to the DC-link (top) and the common dc-link voltage (bottom) of the MPC; no AC-port 1 and a load step-down happens between 0.05 and 0.1 s at the DC-port.

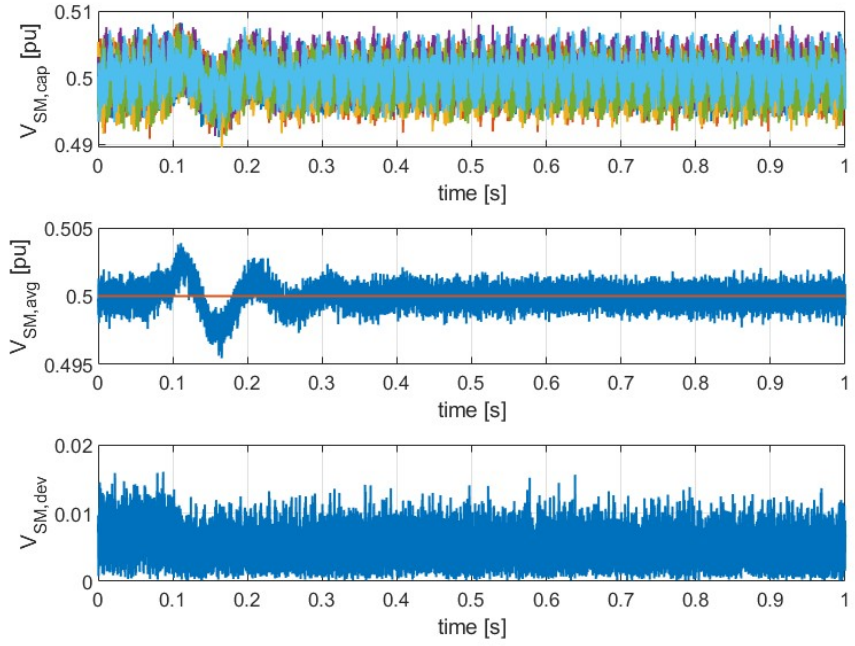


Figure 58: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; no AC-port 1 and a load step-down happens between 0.05 and 0.1 s at the DC-port.

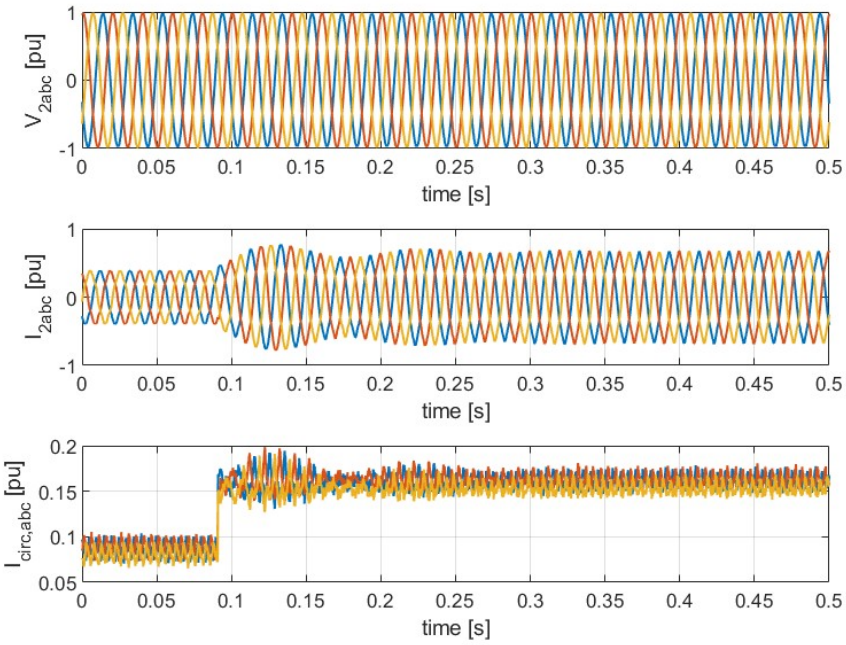


Figure 59: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); no AC-port 1 and a load step-up happens between 0.05 and 0.1 s at the DC-port.

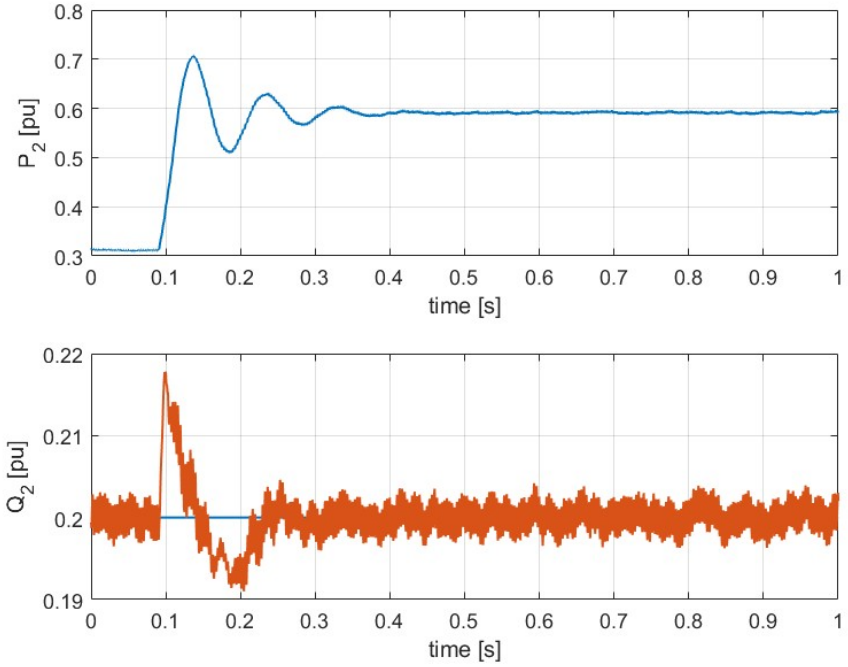


Figure 60: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); no AC-port 1 and a load step-up happens between 0.05 and 0.1 s at the DC-port.

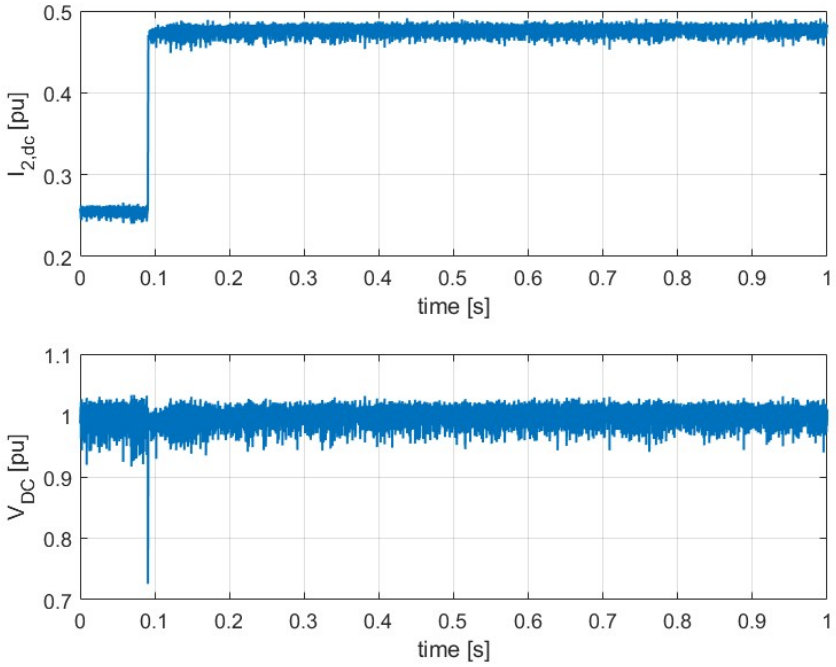


Figure 61: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; no AC-port 1 and a load step-up happens between 0.05 and 0.1 s at the DC-port.

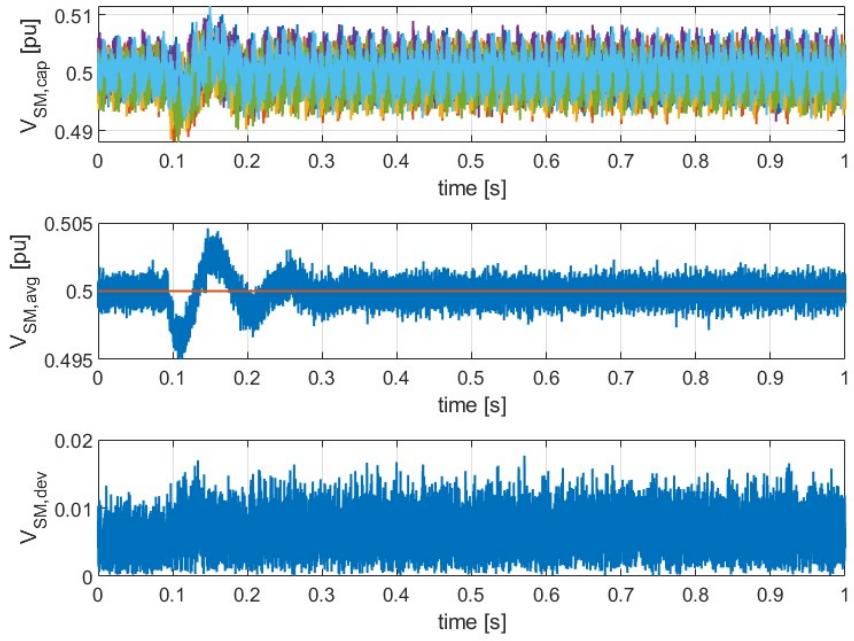


Figure 62: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; no AC-port 1 and a load step-up happens between 0.05 and 0.1 s at the DC-port.

Unbalanced grid-operation: For unbalanced grid-operation as in Fig. 63, a proper controller of the MMC including a negative sequence control is necessary to manage the power exchange at the AC-ports properly. With only the positive sequence control, the impact of unbalanced grid is to affect the proper operation of the converter through oscillation of the power exchange as well as oscillations and unbalances in the SM capacitor voltages (due to unbalanced current exchanges in the AC- and DC-side of the MMC) as shown in Figs. 64 - 66 when an unbalanced grid happens at AC-port 2. This test is performed with no AC-port 1 connected and without the smoothing capacitor on the DC-port.

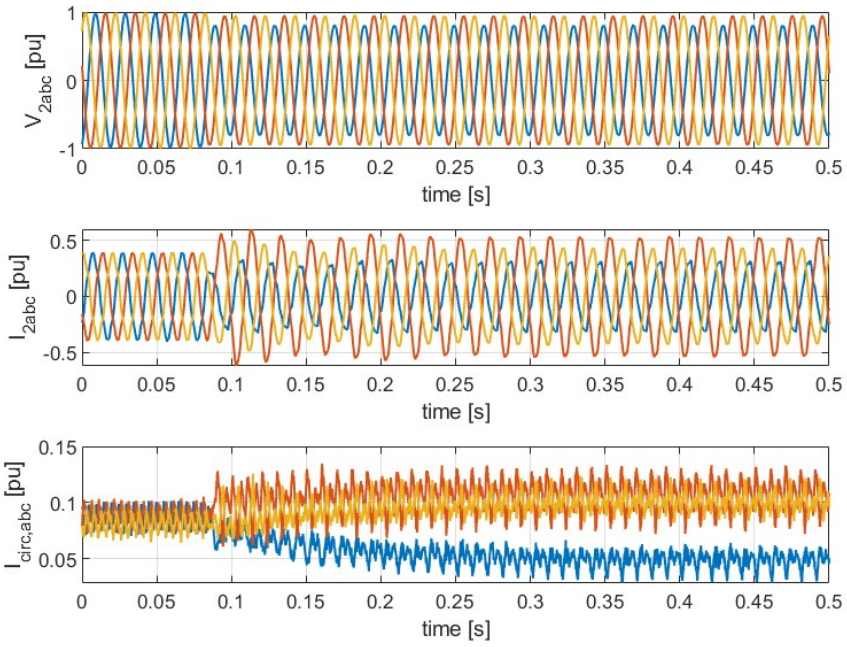


Figure 63: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence AC-side controller is not implemented.

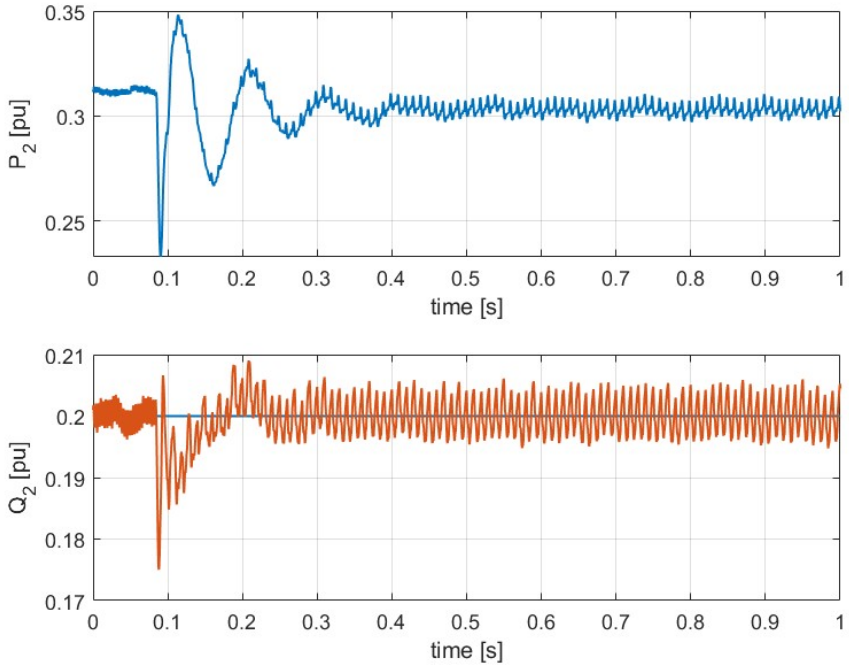


Figure 64: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence AC-side controller is not implemented.

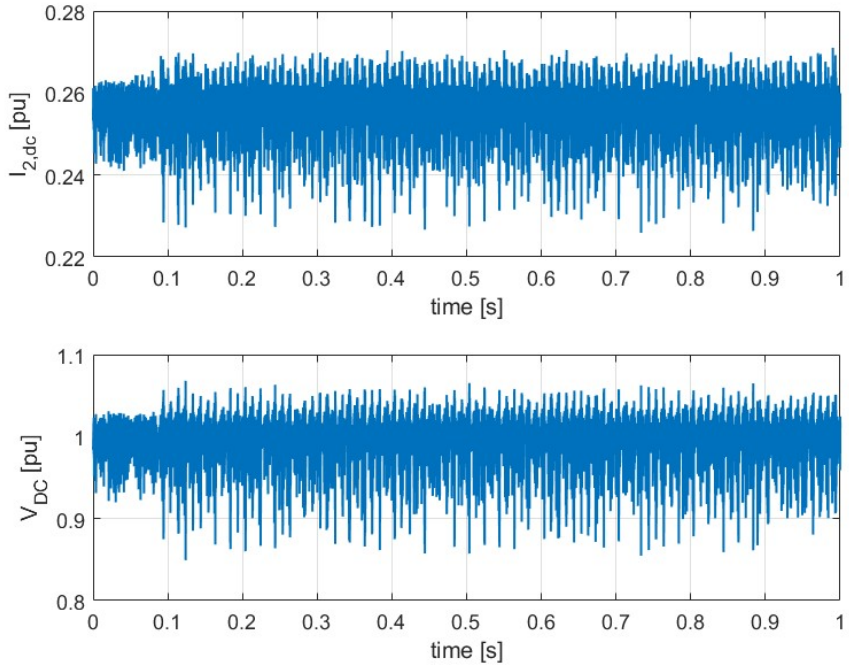


Figure 65: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence AC-side controller is not implemented.

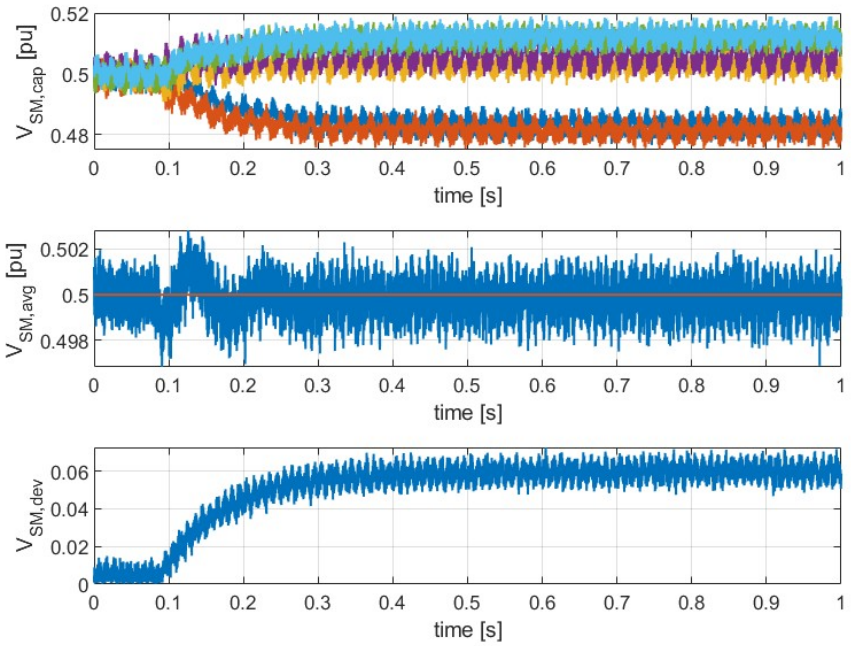


Figure 66: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence AC-side controller is not implemented.

Next, to mitigate the impact of the unbalanced grid on the AC-side, a negative-sequence controller is included for MMC and the tests are performed again for the MPC converter with all ports active and the results are presented in Figs. 67 - 70. Although the negative-sequence controller ensures the grid-side current exchange to be balanced and improves the capacitor voltage unbalance from the previous case, the results show the need for a dedicated unbalance controller as it will be demonstrated next.

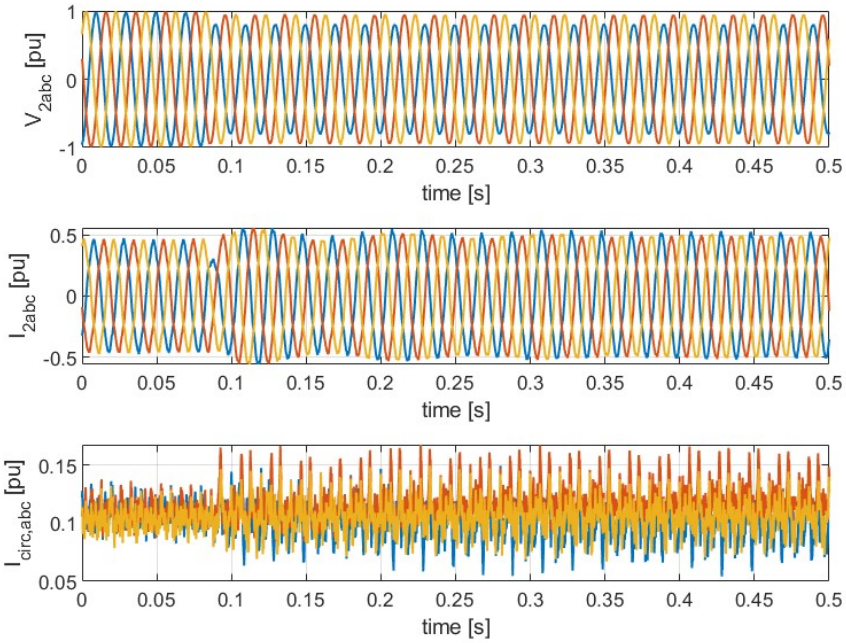


Figure 67: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence AC-side controller is implemented.

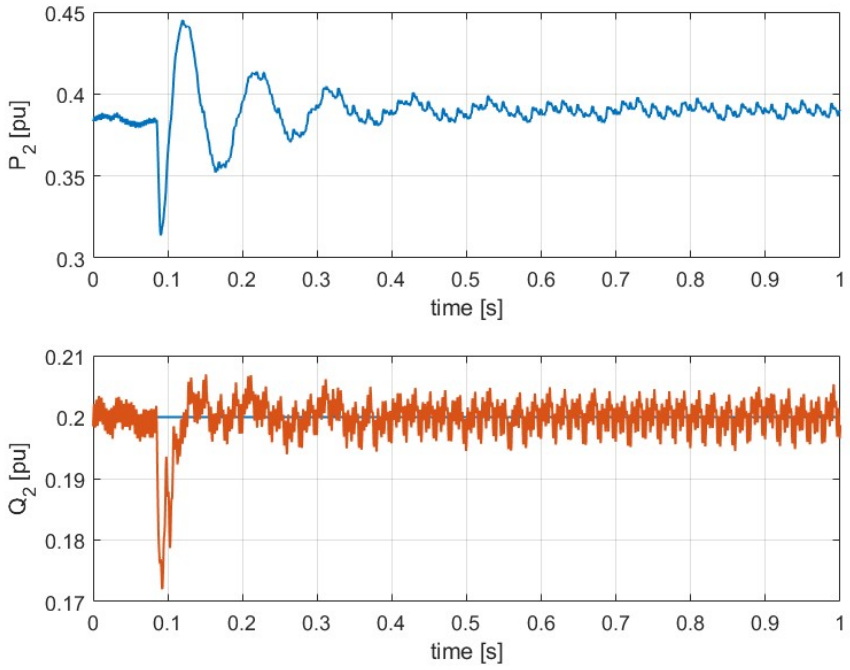


Figure 68: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence AC-side controller is implemented.

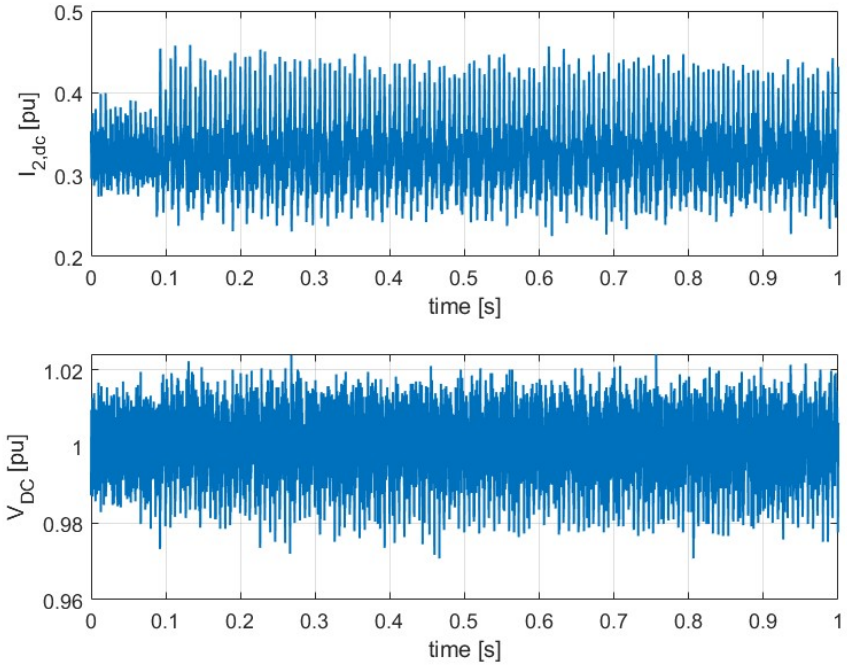


Figure 69: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence AC-side controller is implemented.

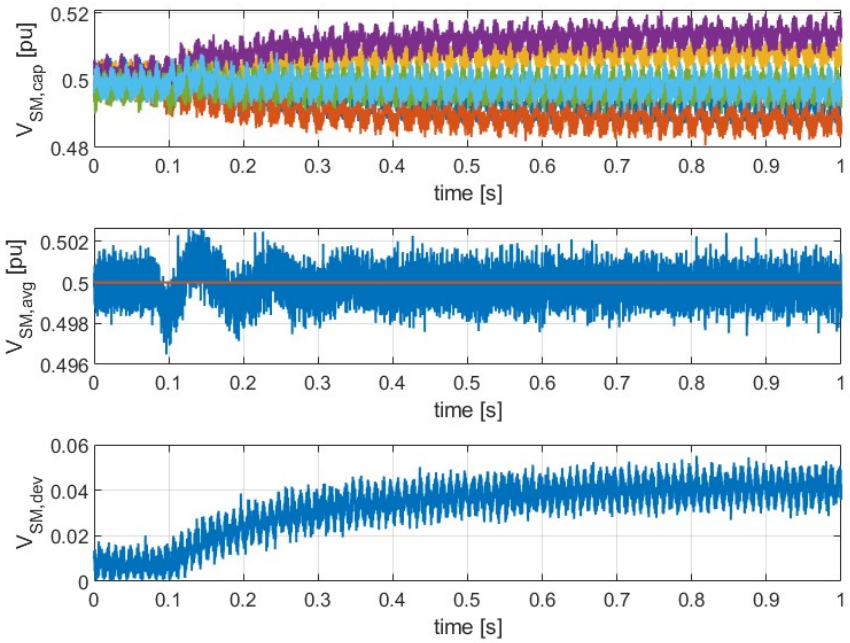


Figure 70: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence AC-side controller is implemented.

Finally, the MPC with all ports active and both negative-sequence and capacitor voltage unbalanced controller implemented, an unbalanced grid voltage dip is applied at AC-port 2. Results in Figs. 71 - 74 shows that the converter operates well in this abnormal operating conditions verifying the effectiveness of the control strategy. In addition, results in Figs. 75 - 78 show that the converter performance is not deteriorated when the unbalanced grid is removed ensuring a successful operation of the converter in normal conditions.

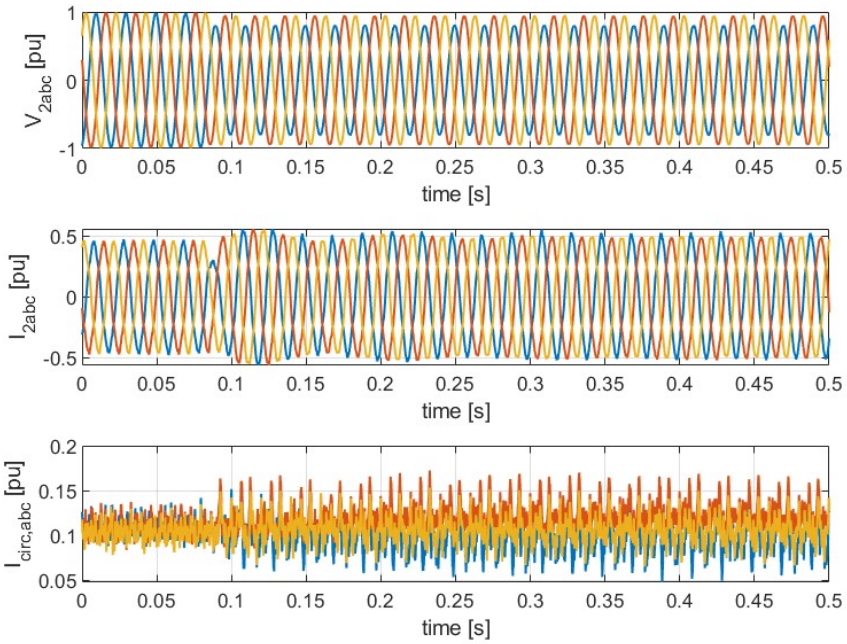


Figure 71: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence and SM-capacitor voltage-unbalance controllers are implemented.

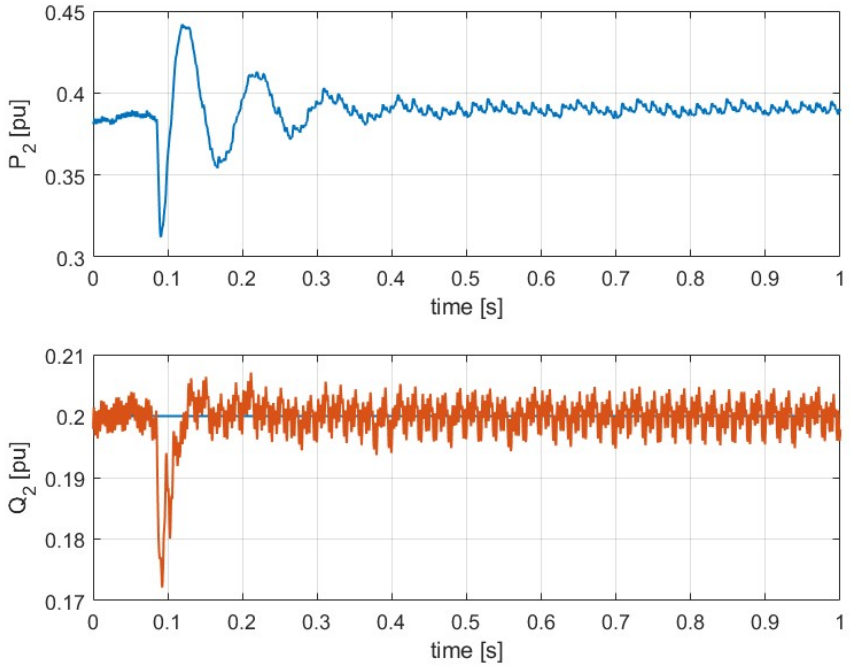


Figure 72: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence and SM-capacitor voltage-unbalance controllers are implemented.

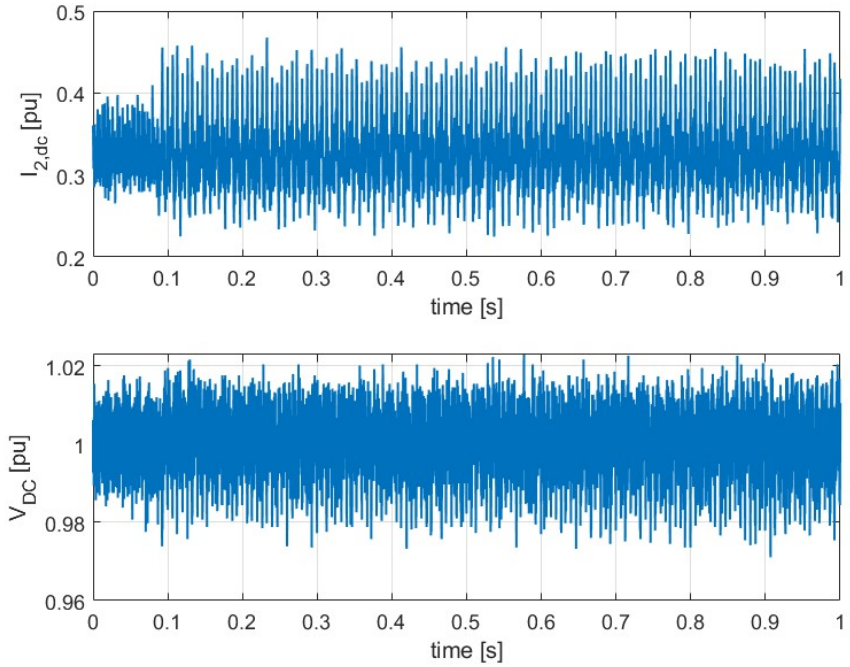


Figure 73: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence and SM-capacitor voltage-unbalance controllers are implemented.

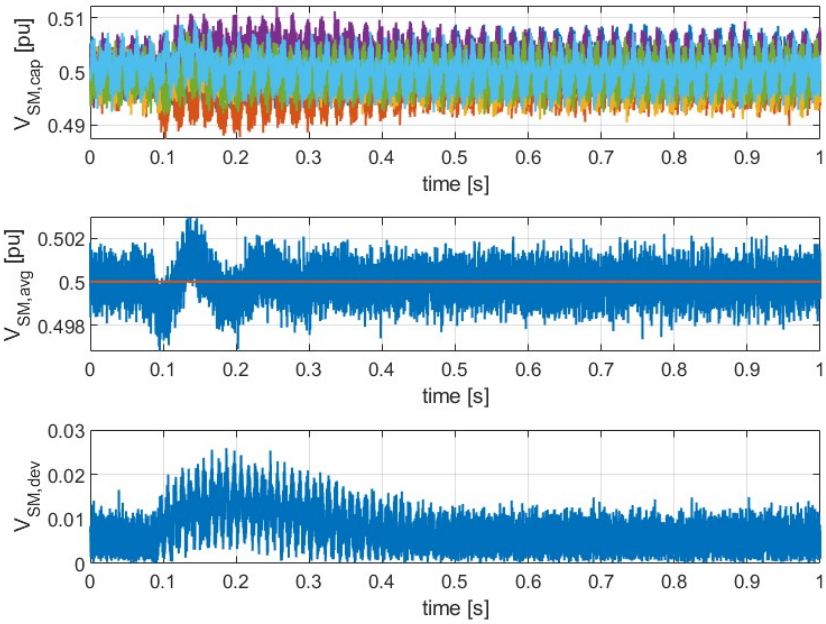


Figure 74: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; an unbalanced voltage dip happens around 0.1 s at AC-port 2 and a negative-sequence and SM-capacitor voltage-unbalance controllers are implemented.

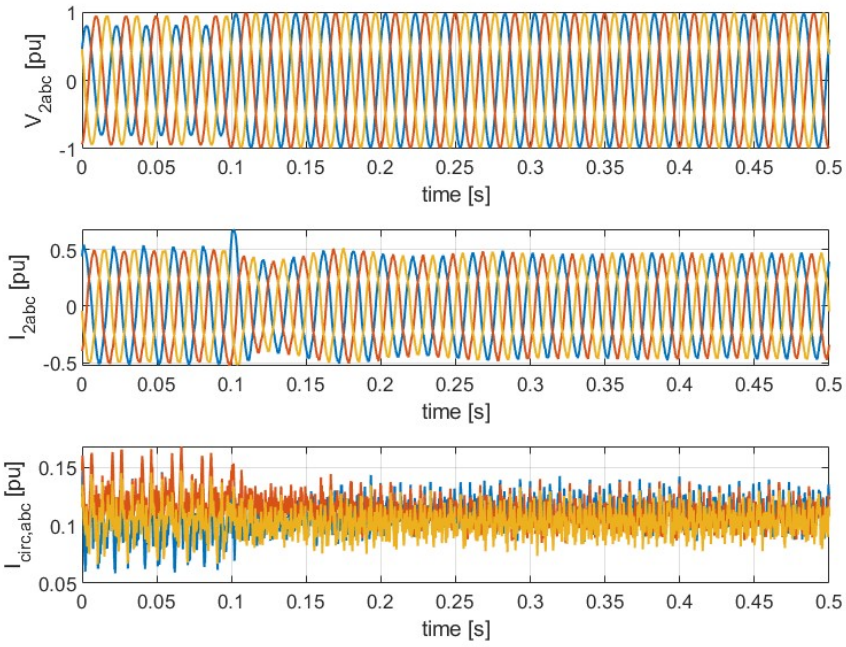


Figure 75: Three-phase grid voltages (top), three-phase grid currents (middle) and three-phase circulating currents inside MMC phase legs at port 2 (bottom); the unbalanced voltage dip is removed around 0.1 s at AC-port 2 and a negative-sequence and SM-capacitor voltage-unbalance controllers are implemented.

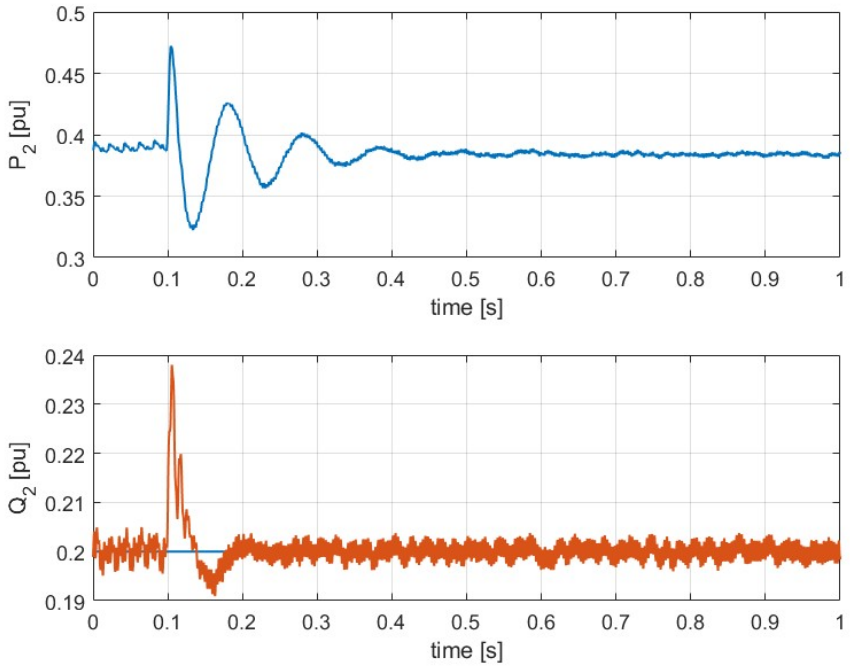


Figure 76: Active power from the grid at port 2 (top) and reactive power from the MMC at port 2 (bottom); the unbalanced voltage dip is removed around 0.1 s at AC-port 2 and a negative-sequence and SM-capacitor voltage-unbalance controllers are implemented.

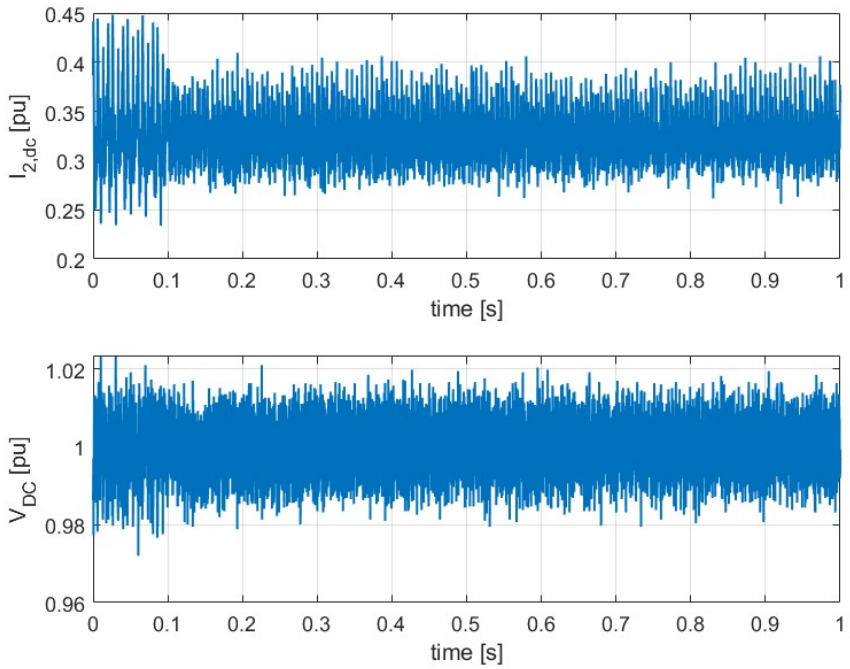


Figure 77: DC current from the MMC to the DC-link (top) and the common DC-link voltage (bottom) of the MPC; the unbalanced voltage dip is removed around 0.1 s at AC-port 2 and a negative-sequence and SM-capacitor voltage-unbalance controllers are implemented.

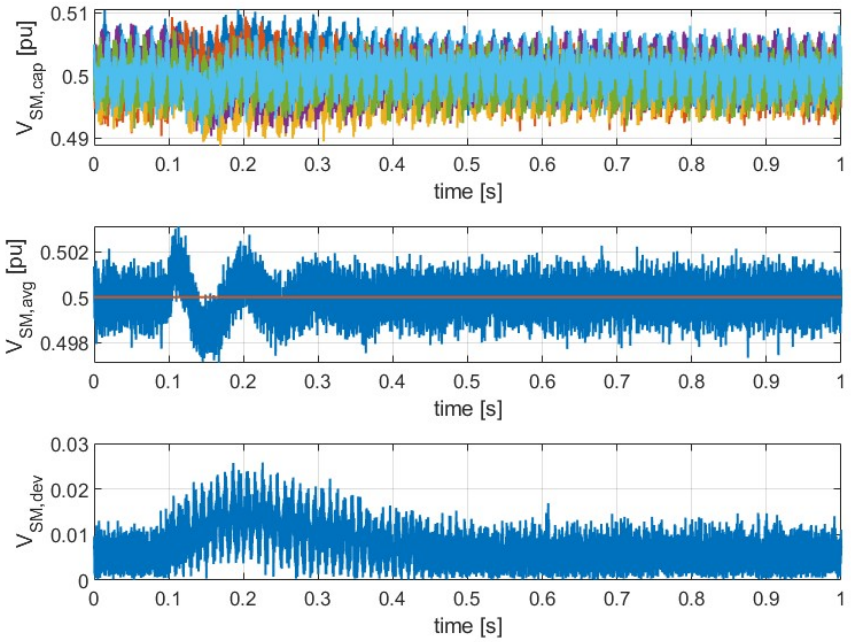


Figure 78: Capacitor voltages of one SM per-arm of the MMC at port 2 (top), average SM capacitor voltage and its reference (middle) and ratio of maximum deviation between the average SM capacitor voltage of each phase-leg of the MMC (bottom) to the nominal SM capacitor voltage; the unbalanced voltage dip is removed around 0.1 s at AC-port 2 and a negative-sequence and SM-capacitor voltage-unbalance controllers are implemented.

6.4 Conclusion

In this section, the partly-isolated topology is validated in the laboratory, where a modified and down-scaled version of the actual topology in terms of the power and voltage levels is developed. The successful operation of the converter topology is demonstrated in a number of tests, where both normal and fault conditions are considered for the tests.

7 Conclusions

In this report, several multiport converter topologies including fully-isolated, non-isolated and partly-isolated ports have been considered in order to compare, evaluate and finally select a topology suitable for medium voltage application. To realize the medium voltage level on the AC-ports, multilevel configuration is adopted using half-bridge and full-bridge cells.

In Chapter 3, a range of feasible topologies were considered to identify the most suitable isolated and partially-isolated topologies to fulfill the enhanced soft-open point (ESOP) application. The winning topologies were chosen to ensure the integration of two medium voltage AC feeder ports with a low voltage energy storage system with as high controllability, efficiency, and robustness as possible. The two winning topologies were then compared in detail for two ESOP cases: one with a larger voltage gain from AC to DC port and one with a lower voltage gain. Component counts were implemented as a proxy for the size and cost of different configurations of the topologies. Low intermediate DC voltage (but with feasible modulation ratio) configurations of the partially isolated topology were capable of operating with a lower number of components than the isolated topology. Detailed qualitative comparisons were also made to quantify the key performance features of each topology for the ESOP application. These features included the impact of port and component failure, control functionality, and design flexibility. The partially isolated topology performed as well or better in all of the performance features other than the ability to handle low voltage DC faults. Considering the results of the component count and the qualitative comparison the partially isolated topology is deemed to be most suitable for the medium to low voltage ESOP application and, therefore, is selected for hardware development and analysis.

A DC-DC converter with a high-frequency transformer provides the isolation needed in the partly-isolated topology selected in the previous chapter. The Triple-active bridge DC-DC converter topology is one of the many options that can be adopted in the configuration. In Chapter 4, the feasibility of achieving a trade-off between zero voltage switching (ZVS) operation and reduced rms current for the triple active bridge converter (TAB) has been demonstrated. Initially, a comprehensive grid search optimization (GSO) is employed to find the minimum rms current within a subset of points that achieve either partial or full ZVS. Subsequently, a multi-dimensional ripple correlation control (MD-RCC) is utilized to optimize a novel cost function that accounts for both rms current and hard switching currents. The results of the MD-RCC search highlight its advantages of being online, model-free, and adaptable to parameter changes online. While the optimization of the new cost function may result in points with slightly higher total rms current compared to the absolute minimum, the primary goal is to balance the total rms current and the hard switching current. This trade-off not only impacts efficiency but also affects EMI noise levels and

the lifetime of the converter. The proposed optimization algorithm is validated through extensive simulation and experimental test cases. Future work could include investigations to improve the practical implementation of the approach and to show the benefits of the achievable operation regimes of converters exploiting the resulting optimal modulation parameters.

In Chapter 5, a comparative analysis of control strategies for a non-isolated MV-MPC based on a FB-MMC topology has been made. The study investigates classical and crossed control approaches, assessing their performance in normal and abnormal conditions. Simulation results demonstrated that while classical control effectively maintains total energy balance, crossed control ensures DC voltage stability, particularly under severe AC fault conditions. With DC faults, only crossed control could ensure a STATCOM behavior. A combined strategy is proposed to leverage the strengths of both approaches, improving the MPC's robustness. The proposed control methods are validated through time-domain simulations using TyphoonSim and further tested in a CHIL setup, confirming their practical feasibility. Finally, it should be mentioned that the conclusions obtained with AC faults can also be applied to HB-MMCs topologies.

Finally in Chapter 6, the partly-isolated topology selected in Chapter 3 is validated in the laboratory. The setup represents a modified and down-scaled version in power and voltage levels of the actual topology. As such, a number of dynamic and steady-state tests both in normal conditions (generation and load changes) and fault conditions (voltage dips, port disconnections) are tested validating the successful operation of the prototype.

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